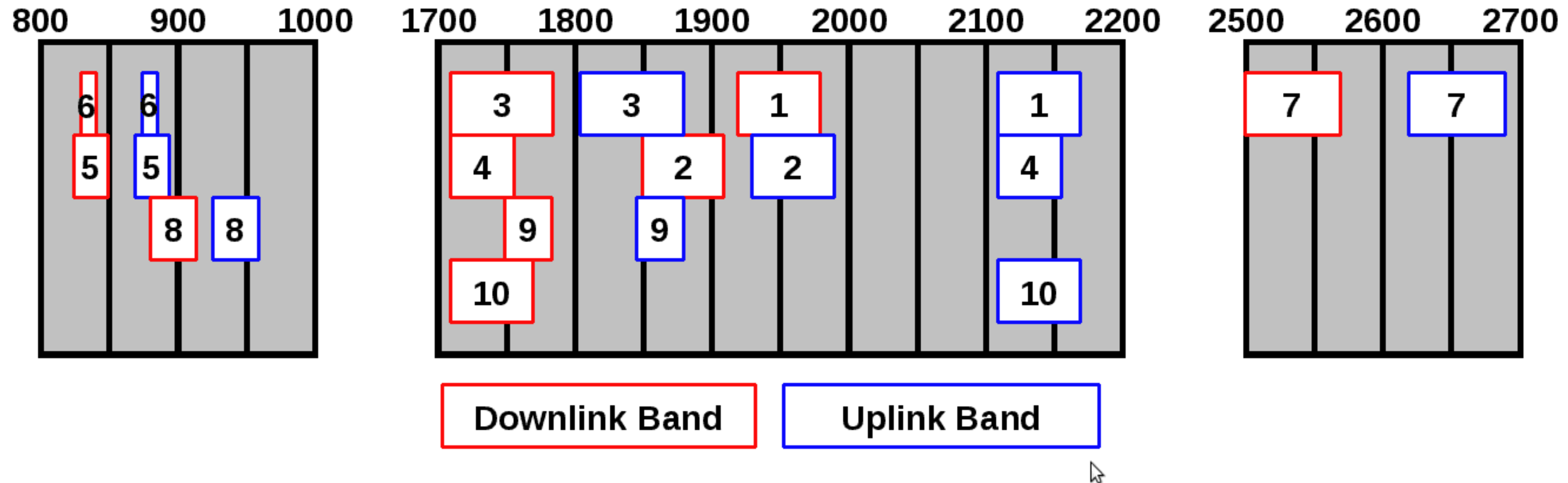

Direct-Conversion WCDMA Transmitter with -163dBc/Hz Noise at 190MHz Offset

Christopher Jones, Bernard Tenbroek, Paul Fowers,
Christophe Beghein, Jonathan Strange,
Federico Beffa, Dimitris Nalbantis

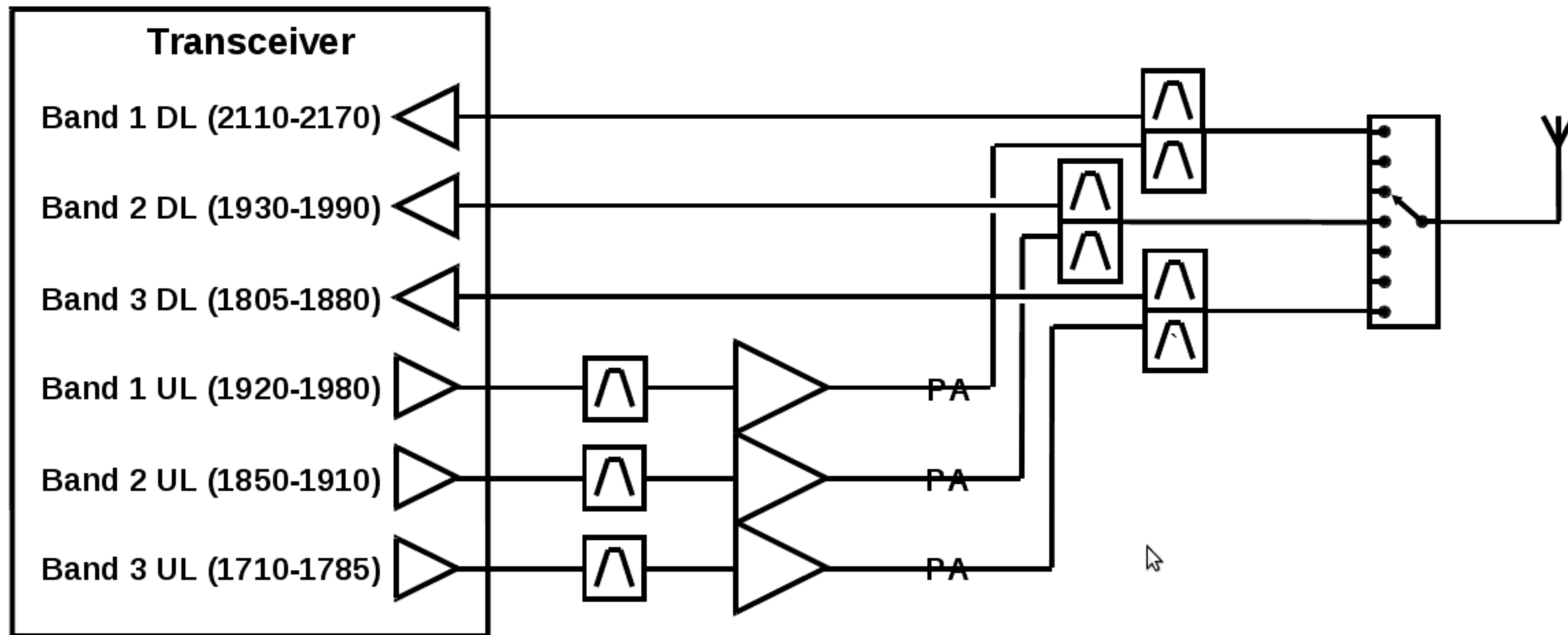
Analog Devices, Kent, United Kingdom

WCDMA Spectrum Available



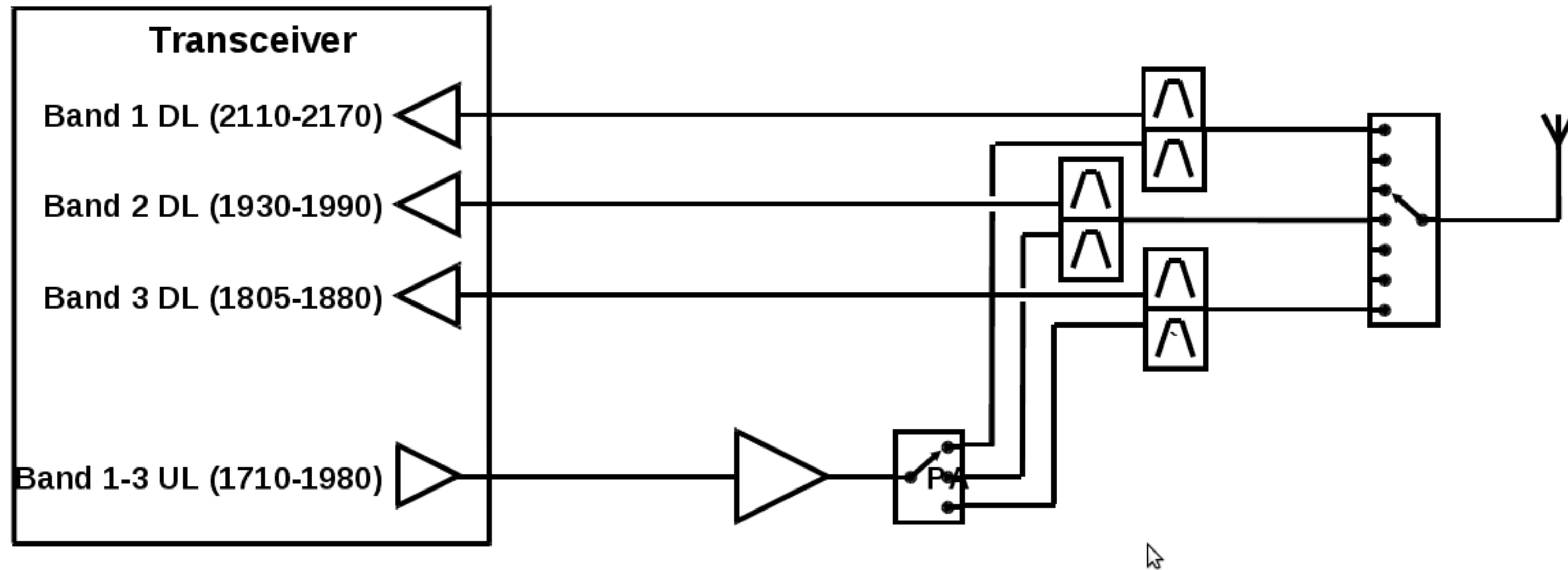
- 10 WCDMA bands now defined by 3GPP
- Most popular today is tri-band 1+2+5
- Emerging interest in bands 4/10, 3/9 and 8

Traditional Multi-Band WCDMA Front End



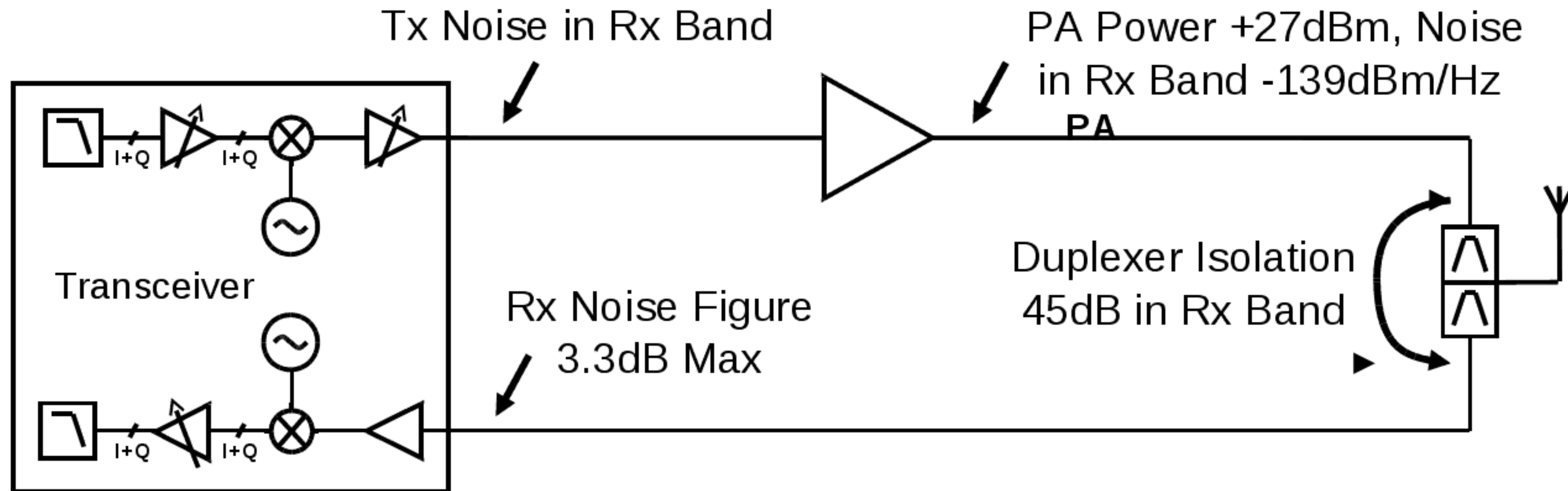
- Separate Tx SAW filters and PAs for each band
- Multi-band designs are large and expensive

Broadband Tx WCDMA Front End



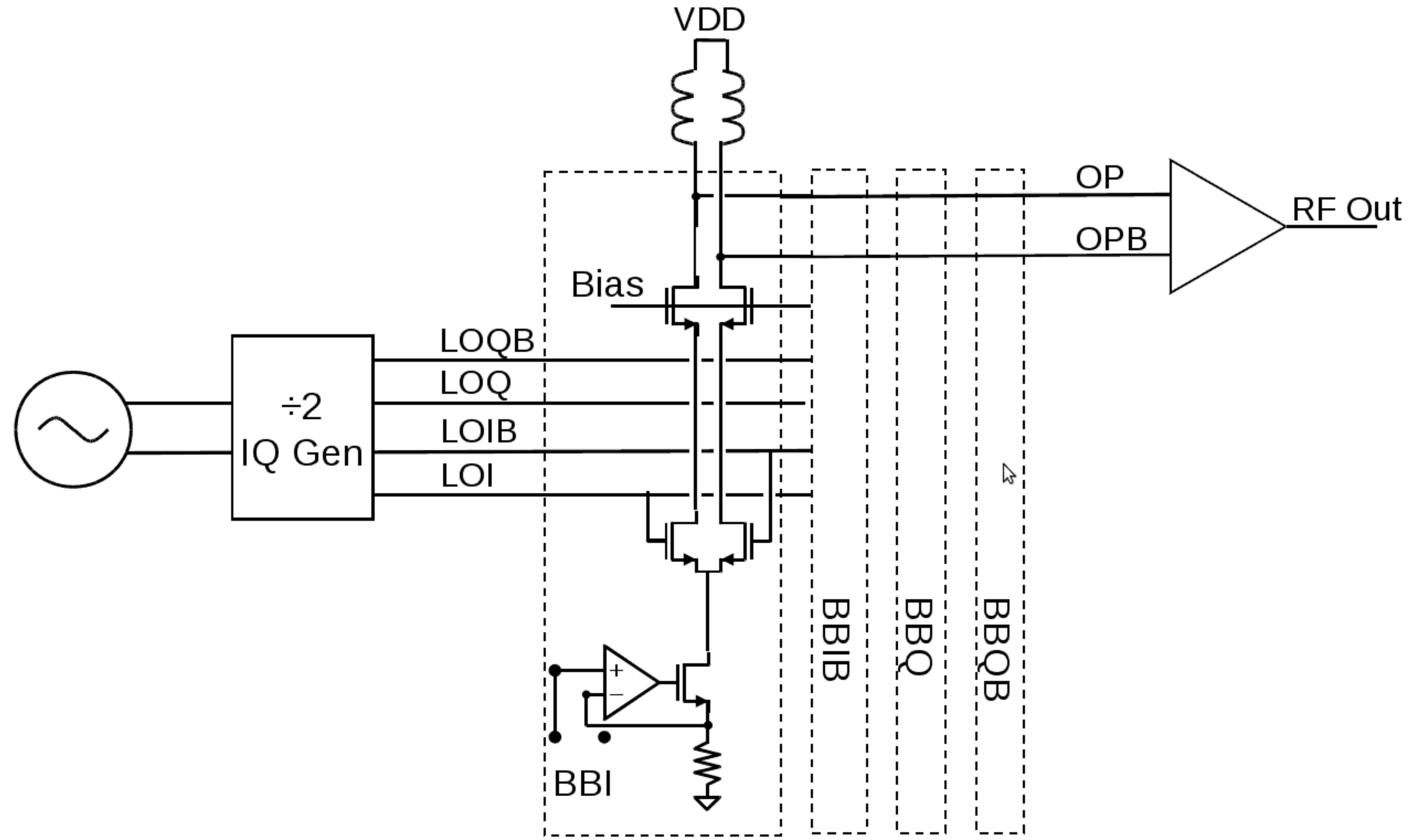
- Allows use of multi-band PAs
- Reduced incremental cost for additional bands
- Enables multi-mode PAs and tuneable filters

Tx Noise Requirement

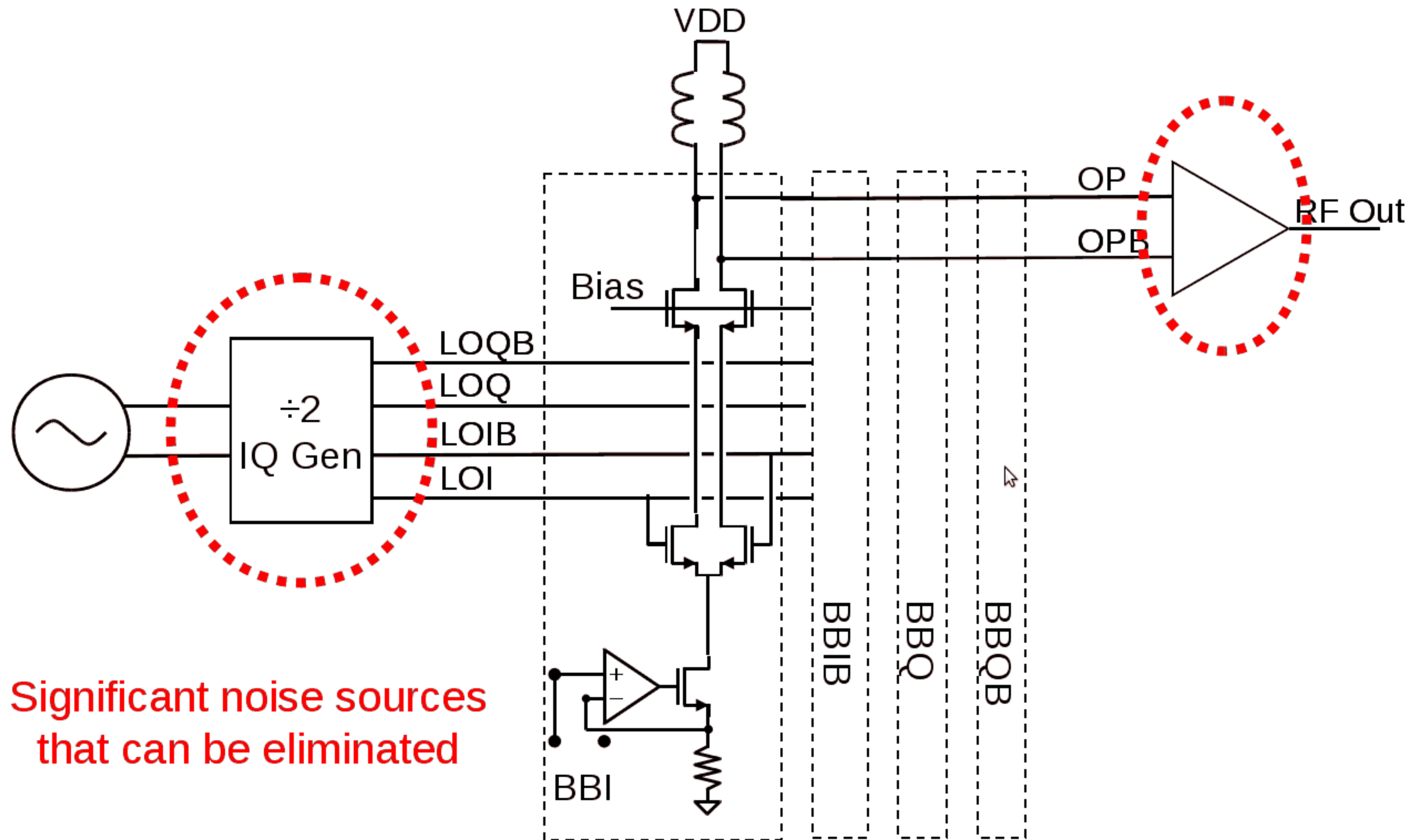


- State of the art PA has -166dBc/Hz noise in Rx band
- Duplexer trend is for smaller size not better isolation
- To keep Rx NF including Tx noise to less than 4dB need Transceiver Tx Noise in Rx Band of **-162dBc/Hz**

Conventional Homodyne Transmitter

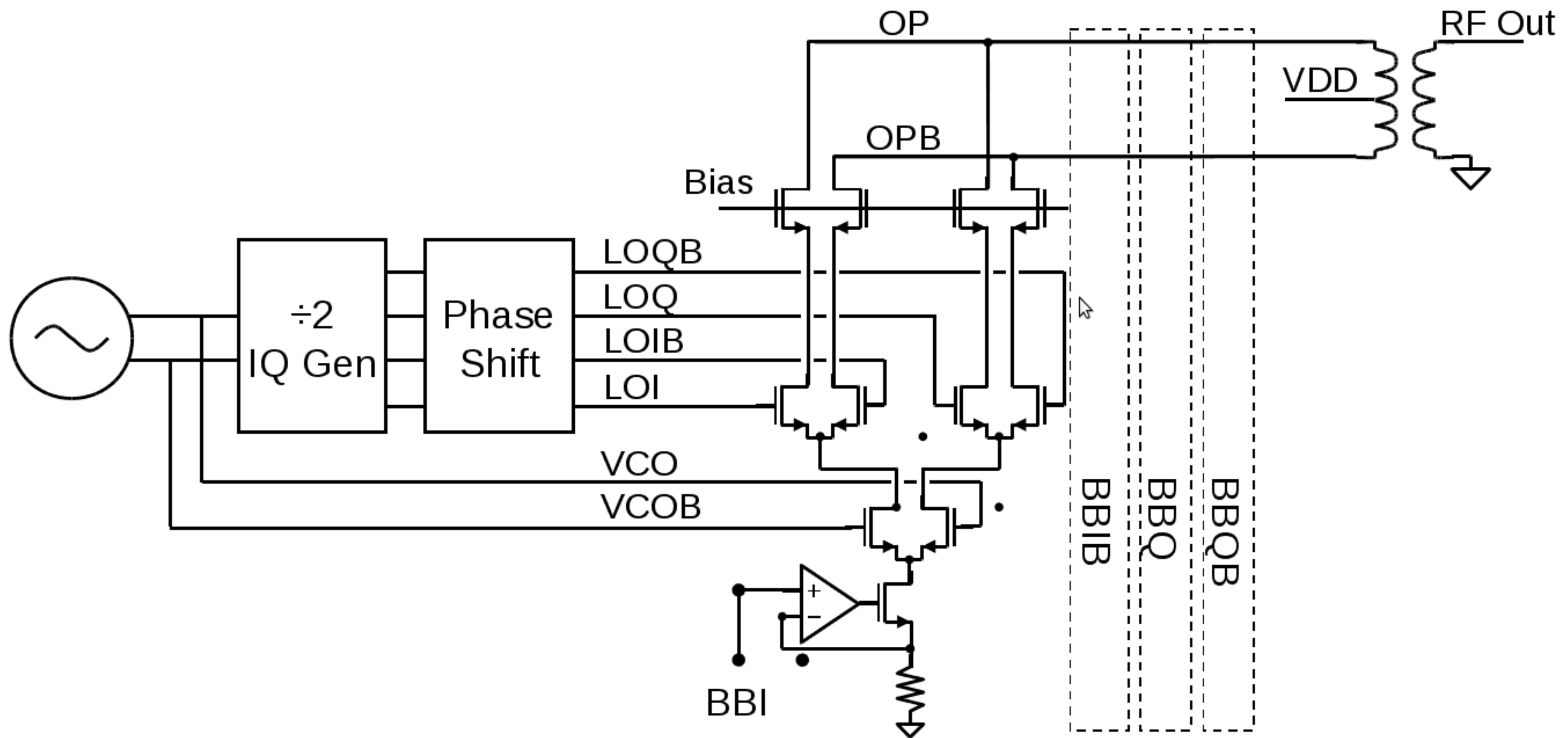


Conventional Homodyne Transmitter



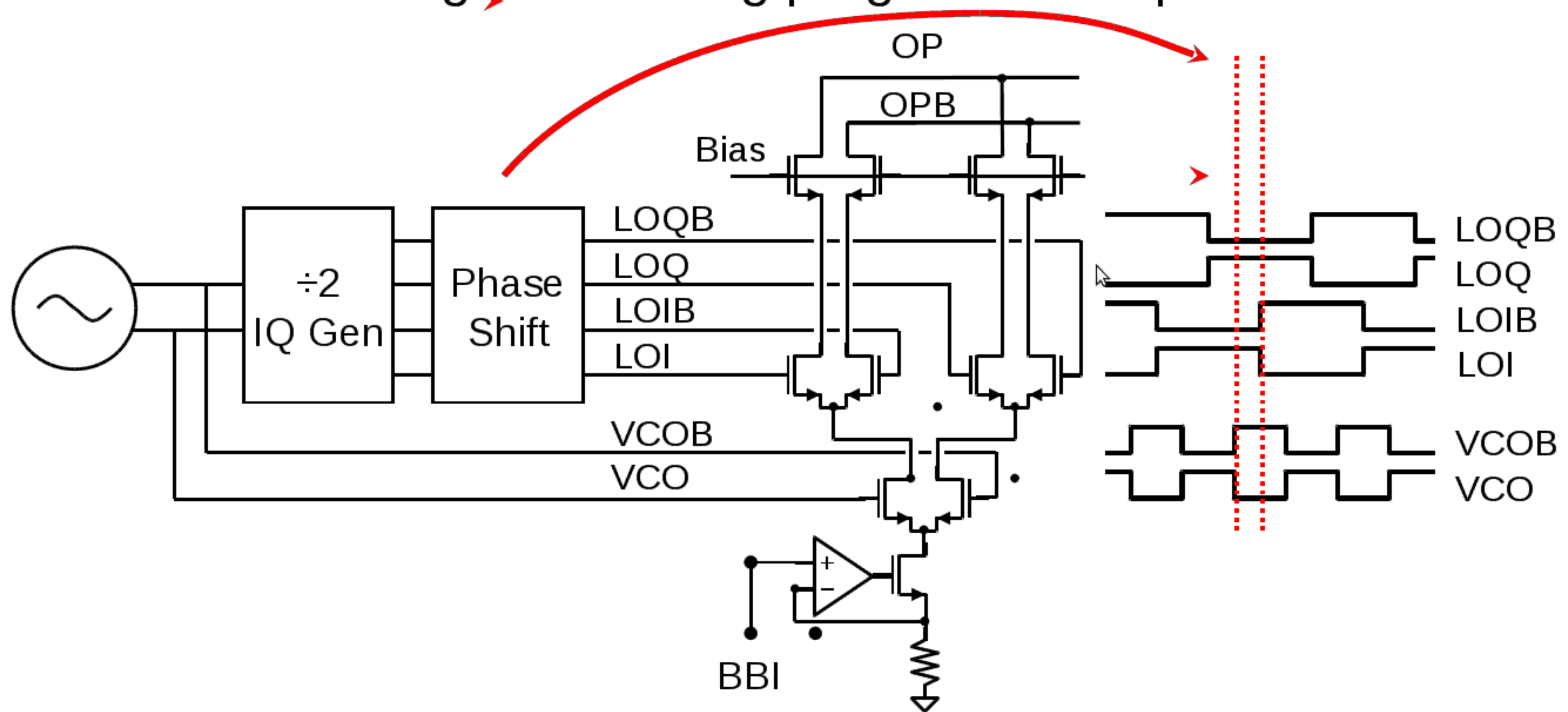
Low Noise Homodyne Modulator

- Additional VCO switch to suppress LO tree noise
- No separate driver stage

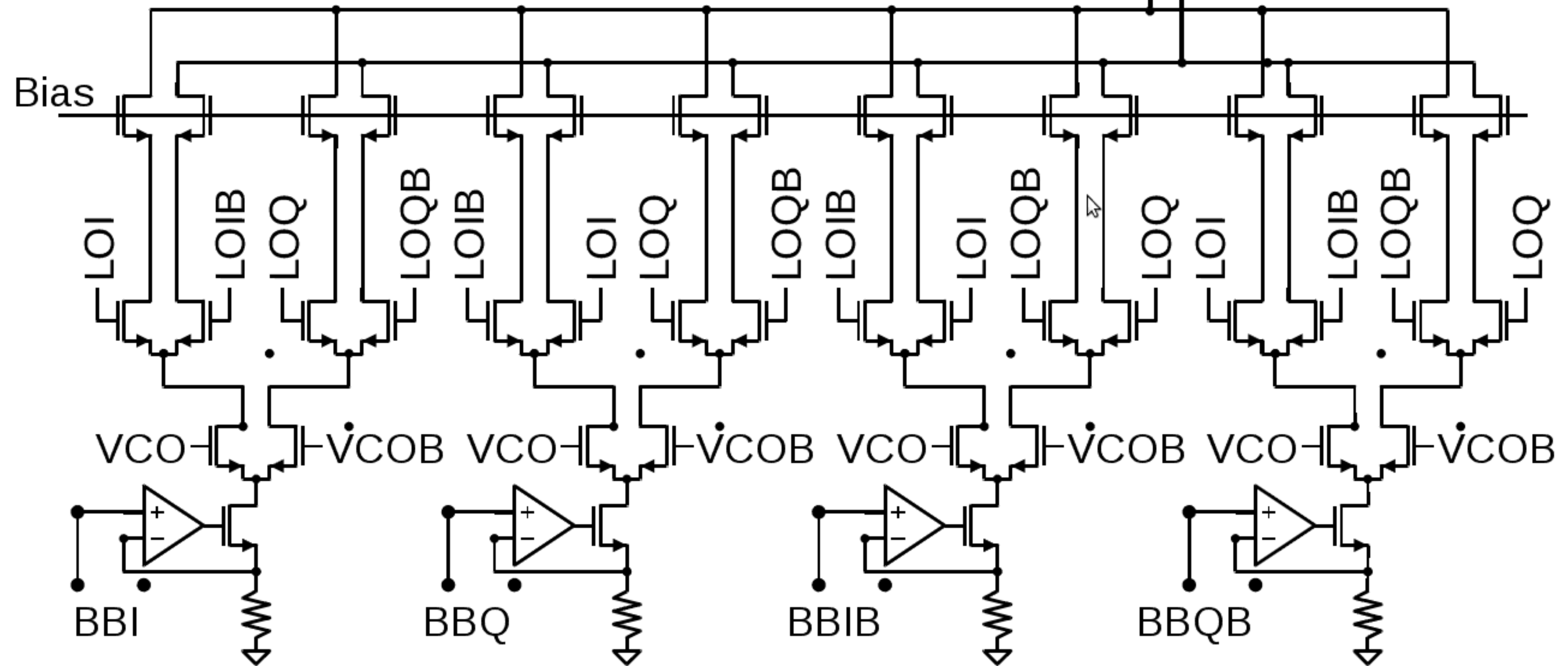
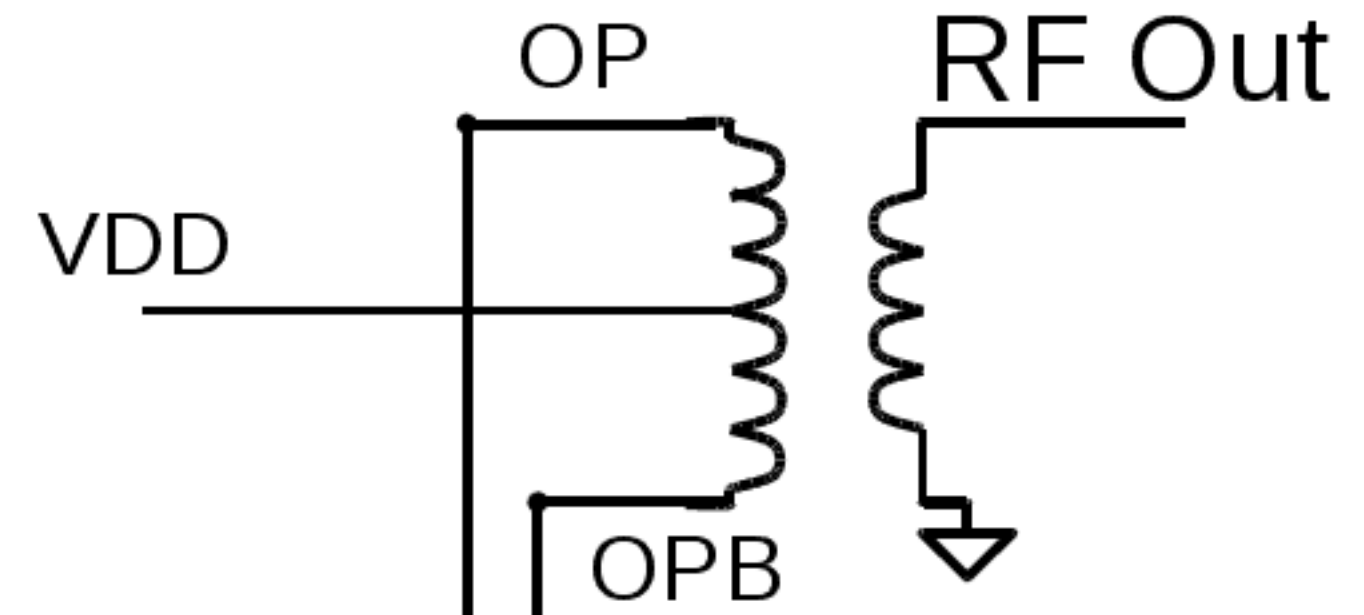
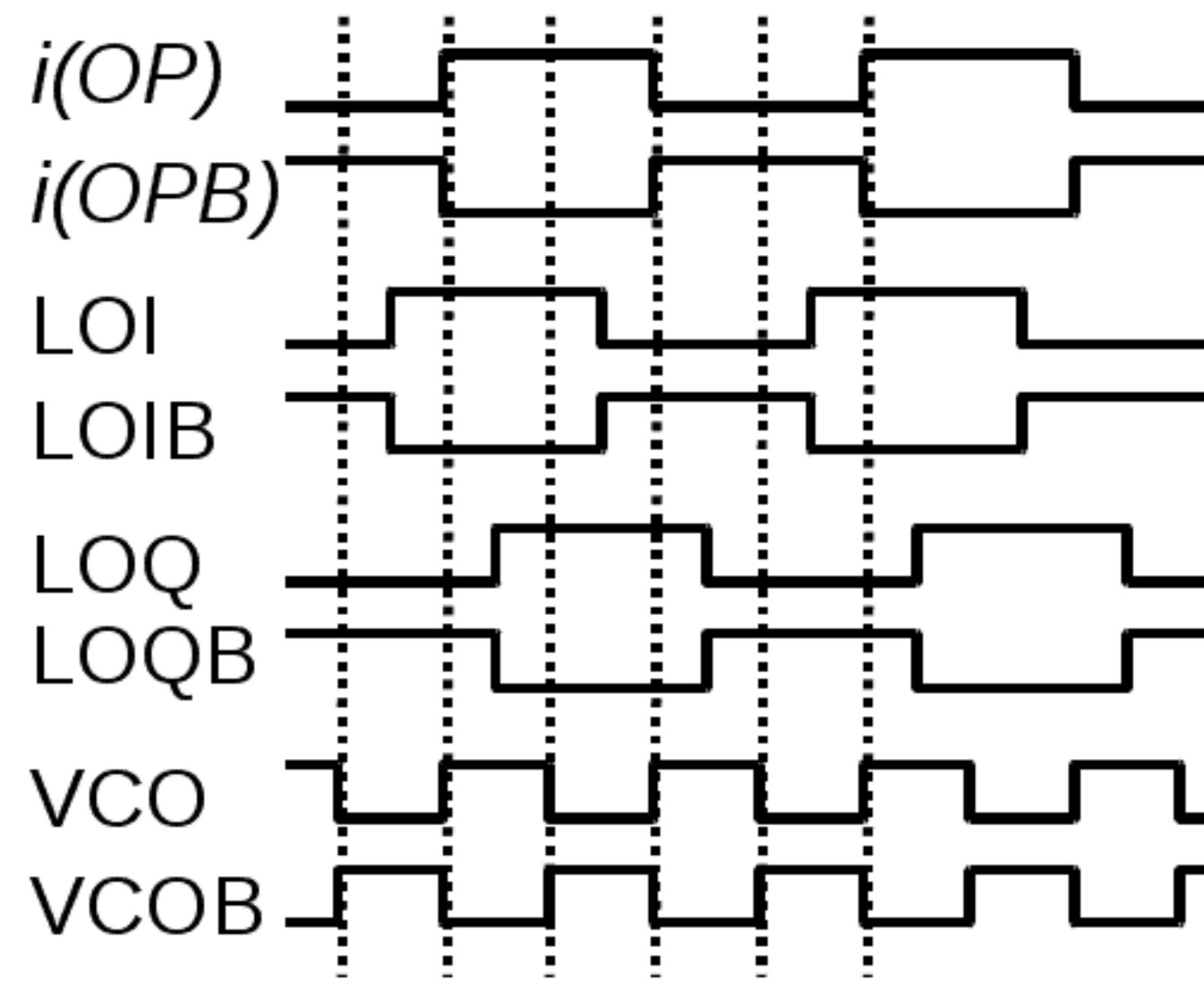


Principle of Operation

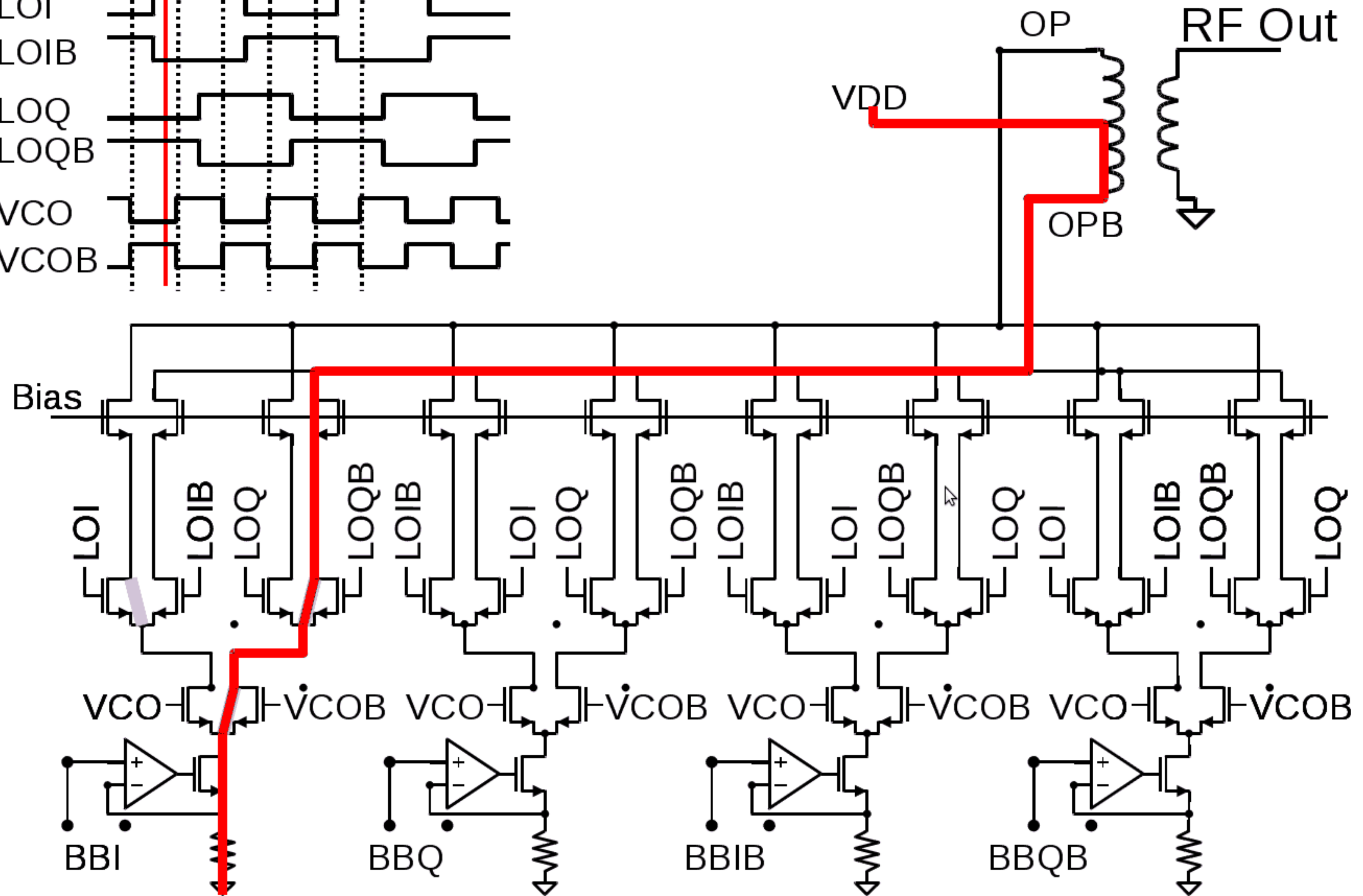
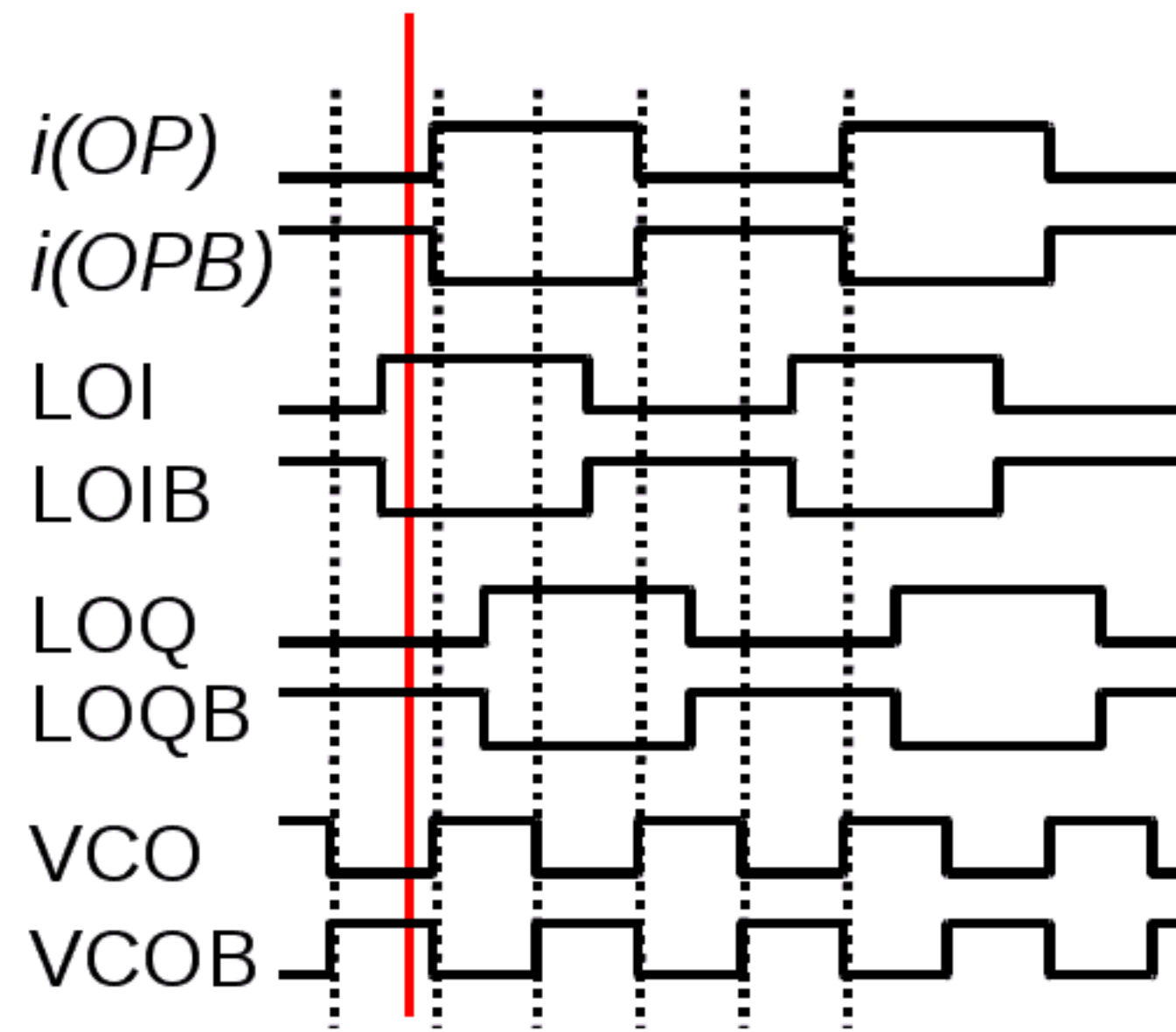
- LOI edge occurs when all current is through LOQ pair
- Align LO edge in centre of correct VCO half period
- Automatic alignment using programmable phase shift



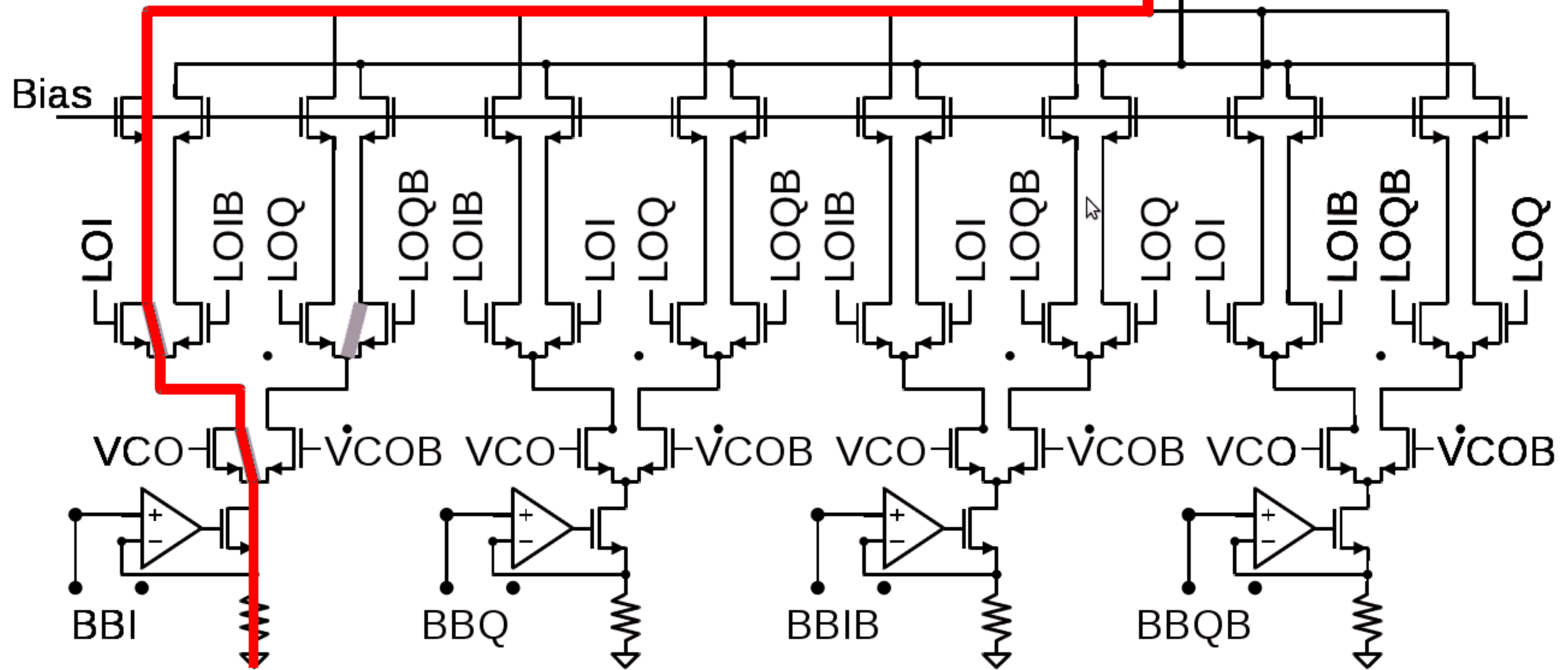
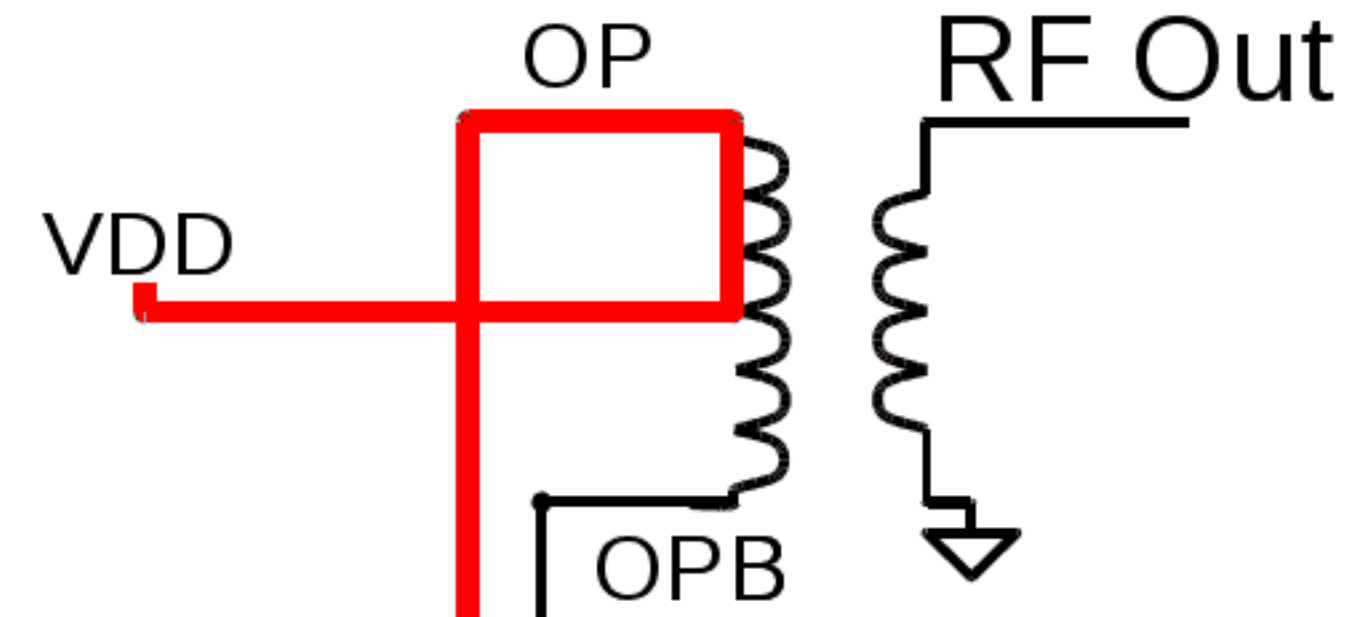
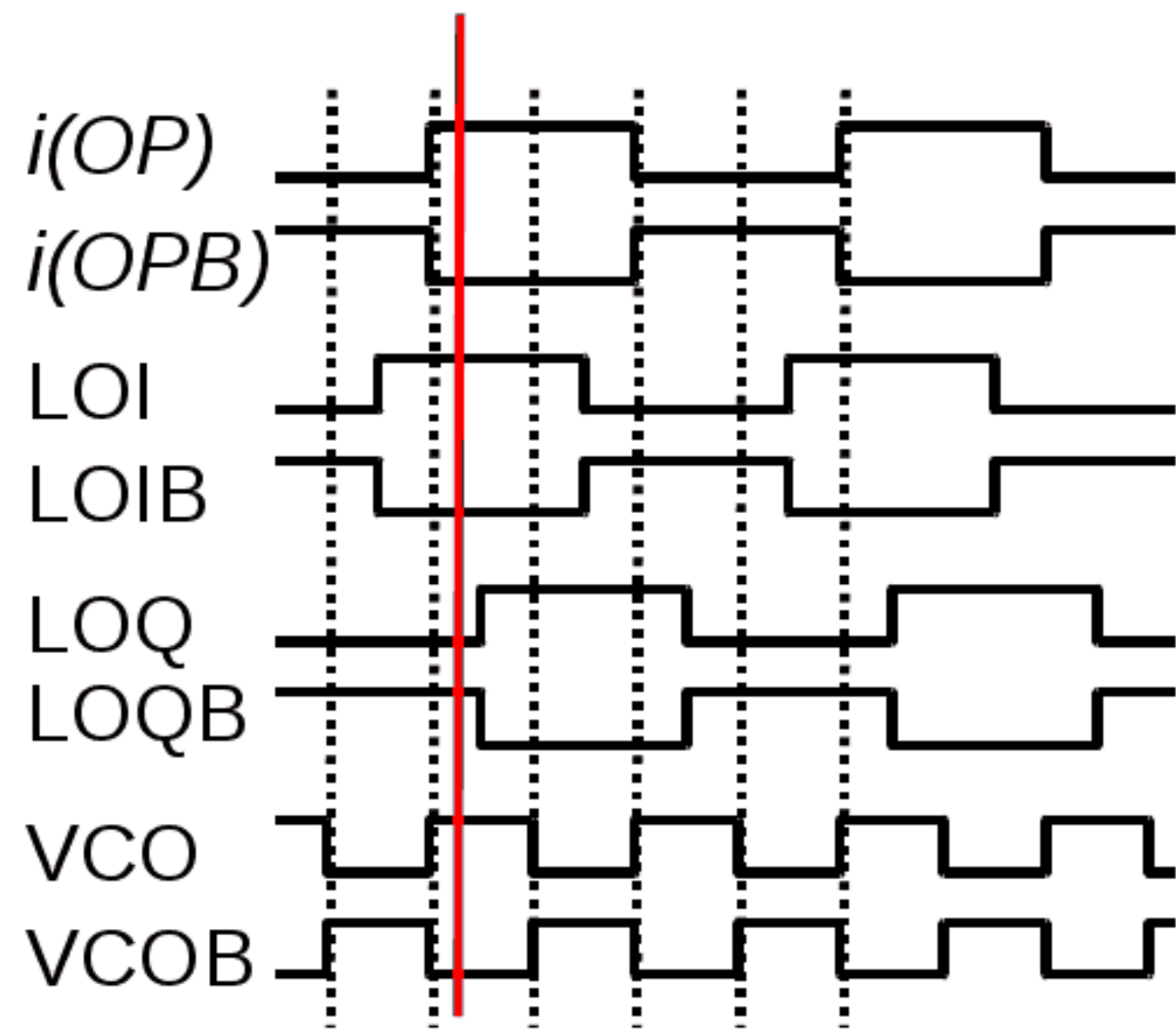
Switching Sequence



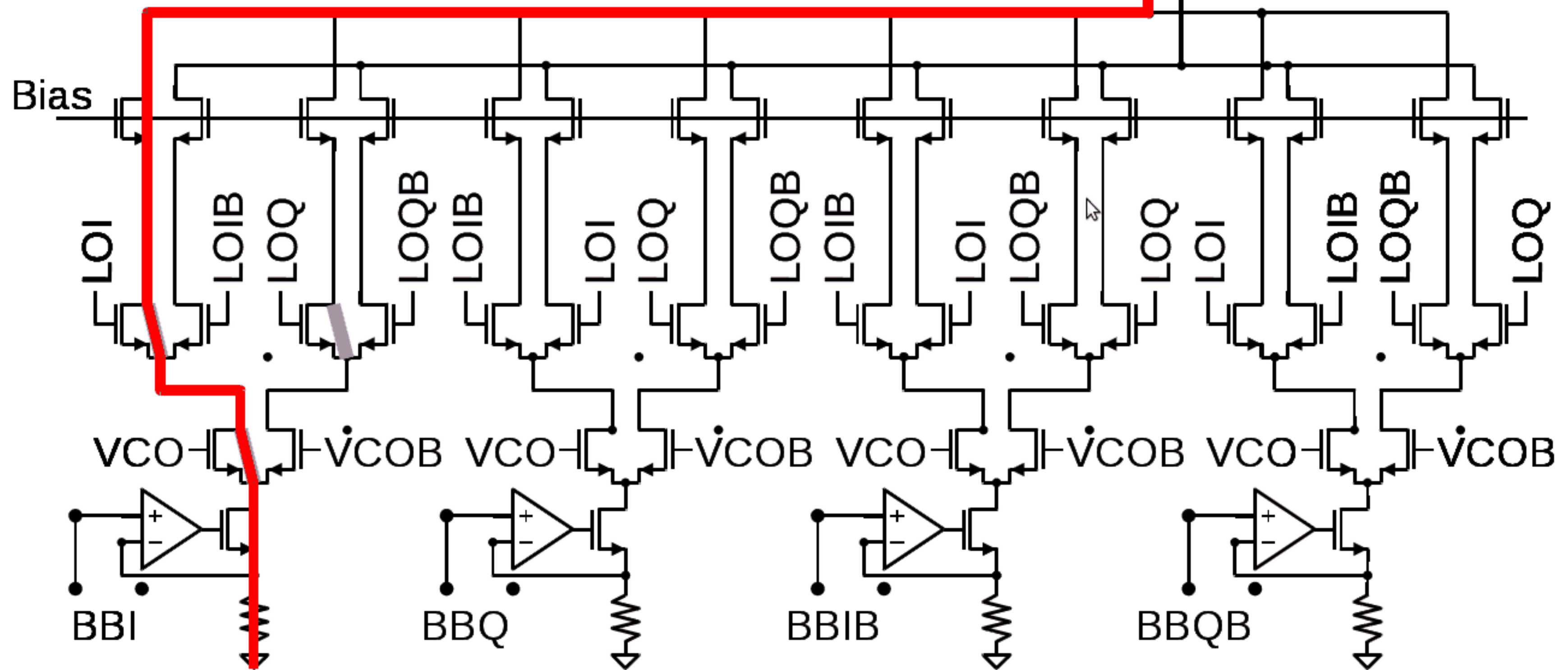
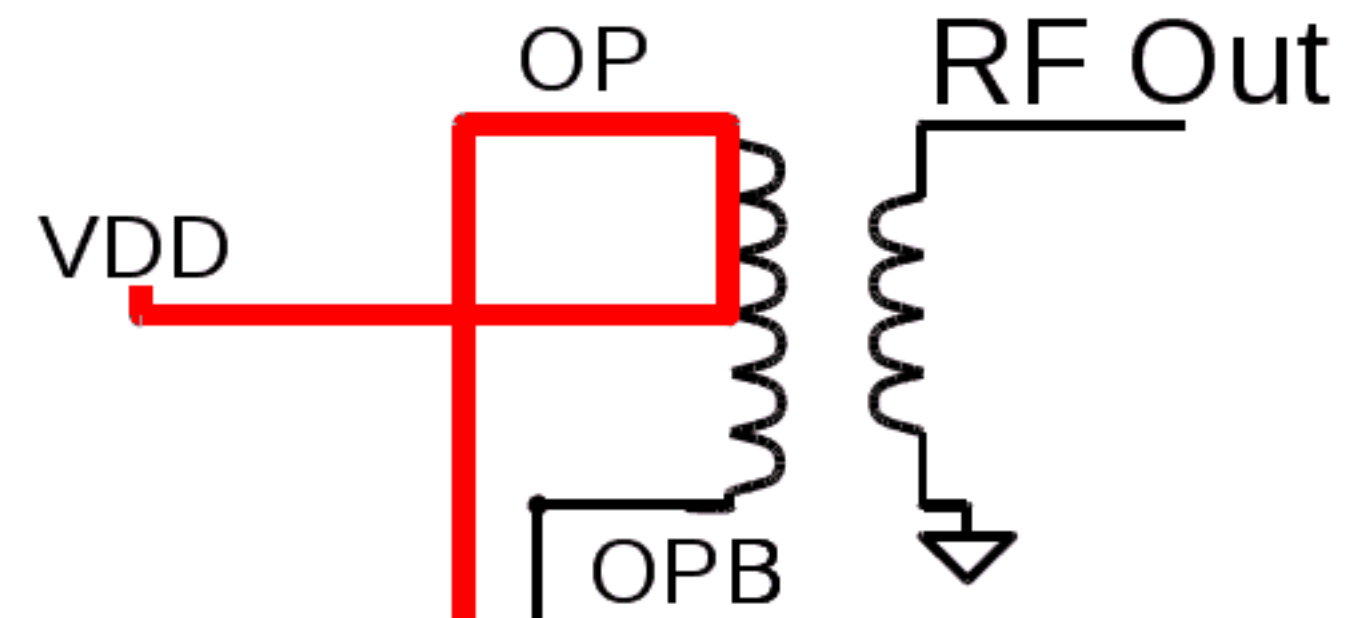
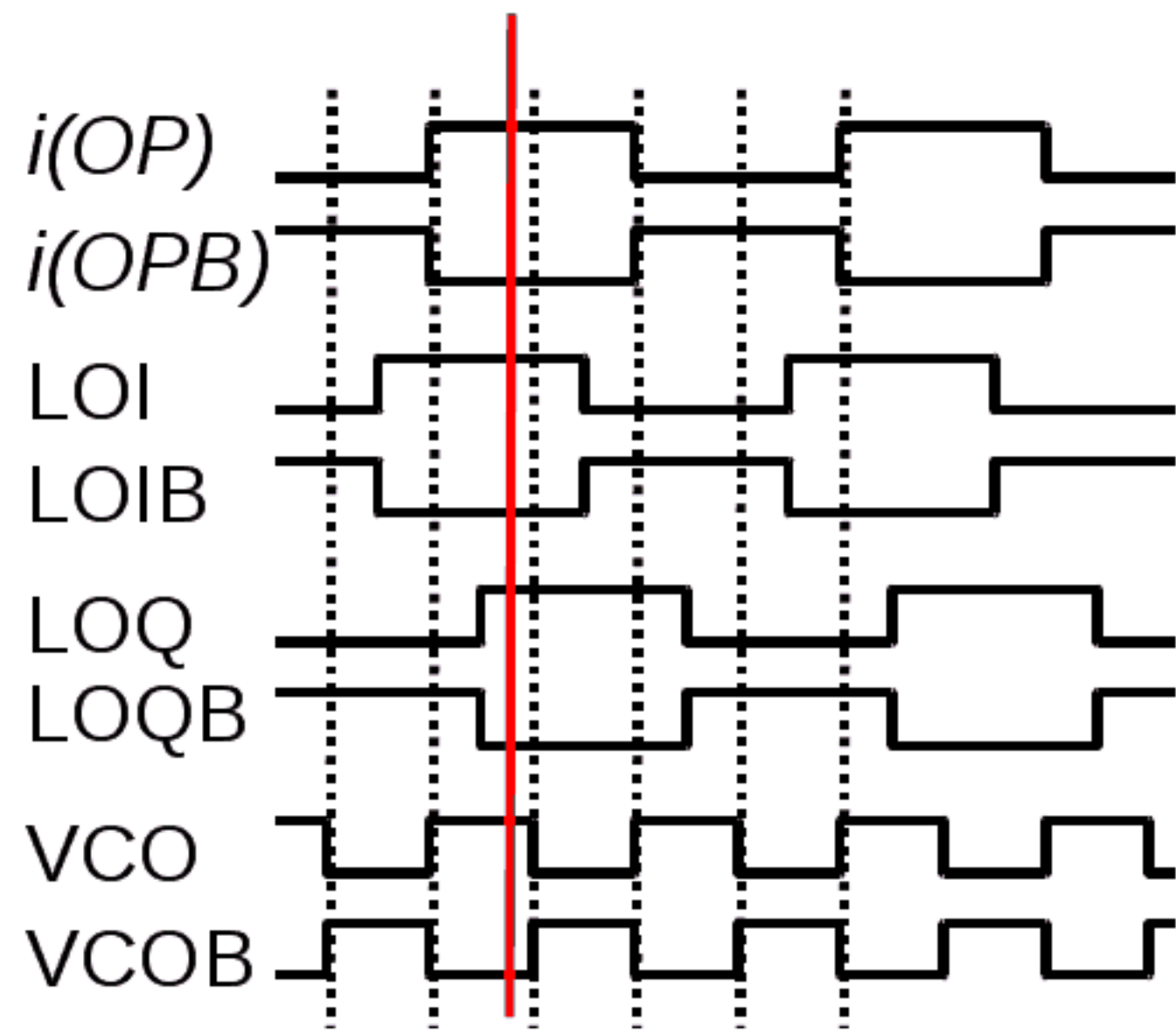
Switching Sequence



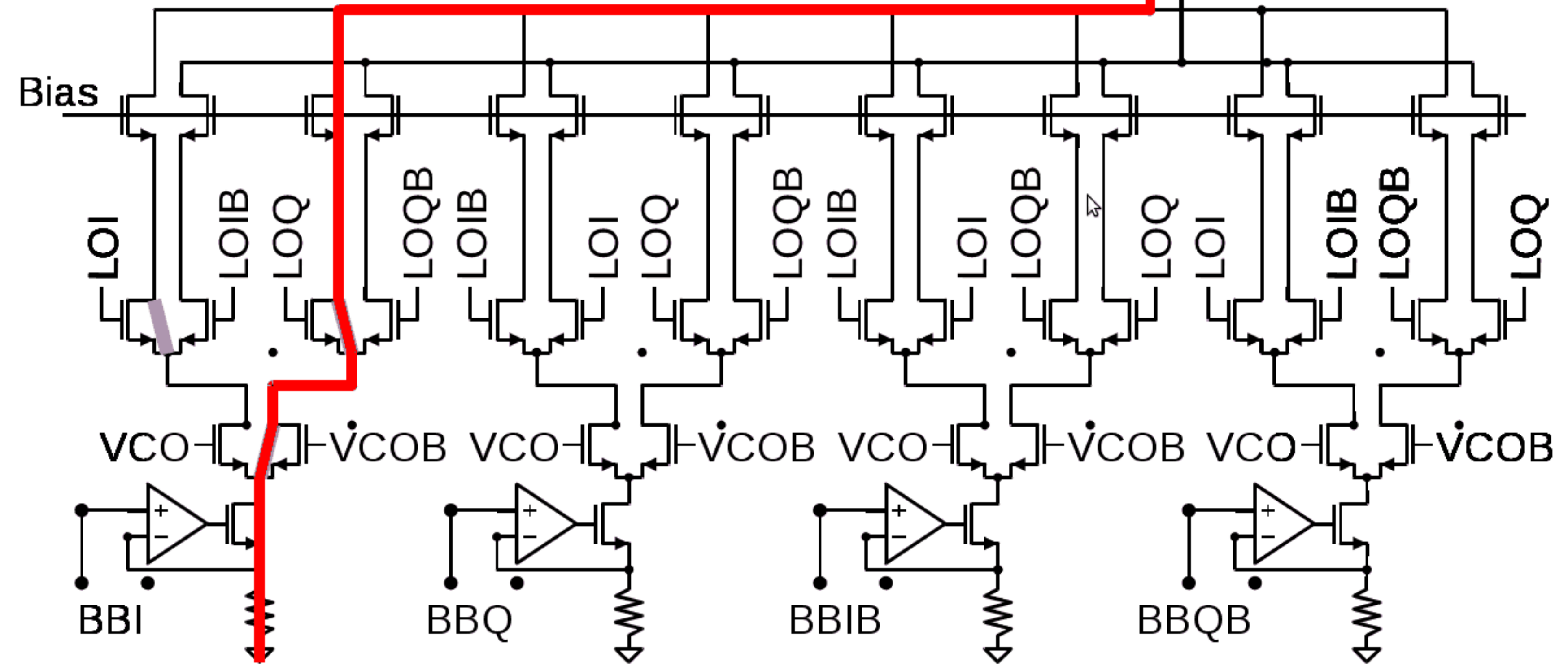
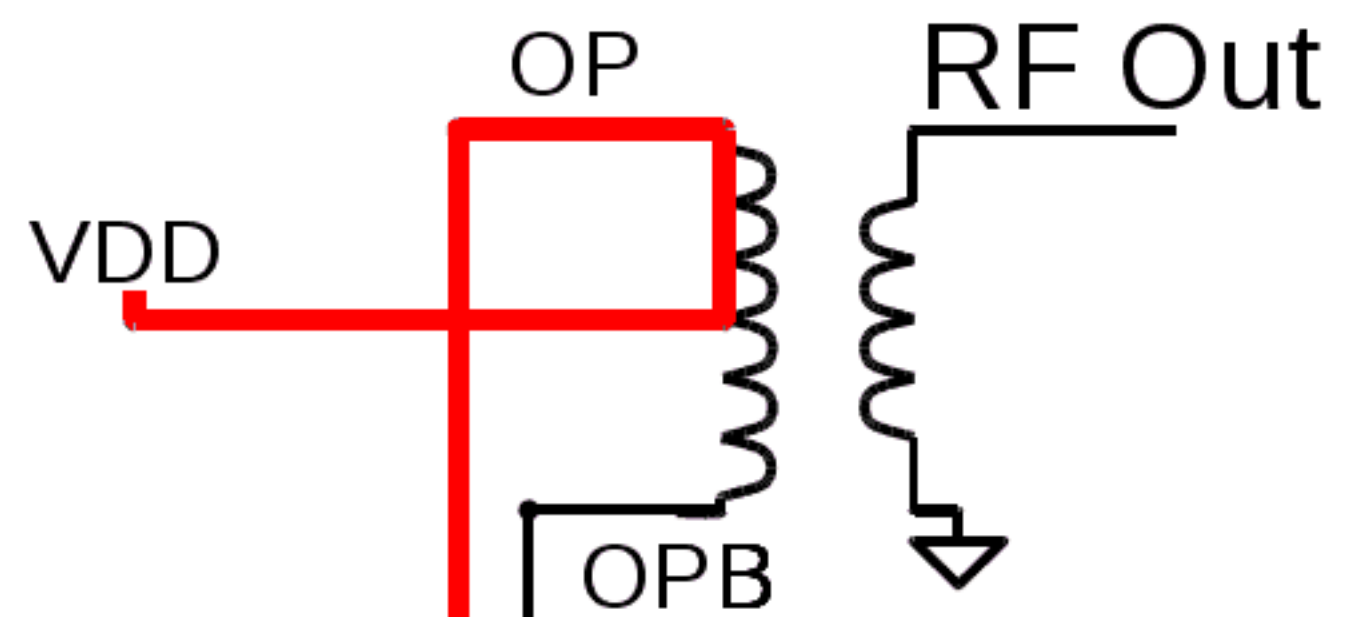
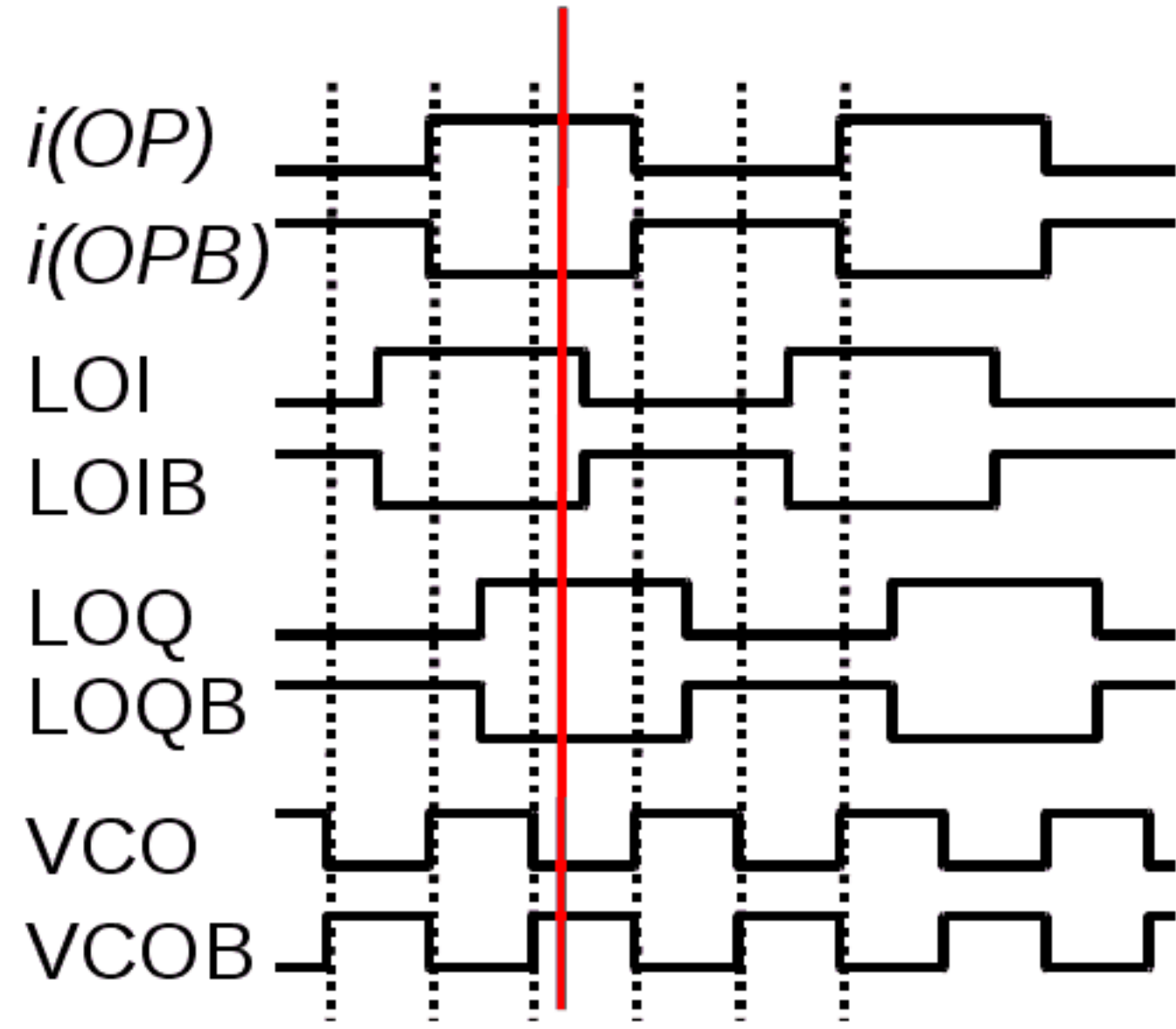
Switching Sequence



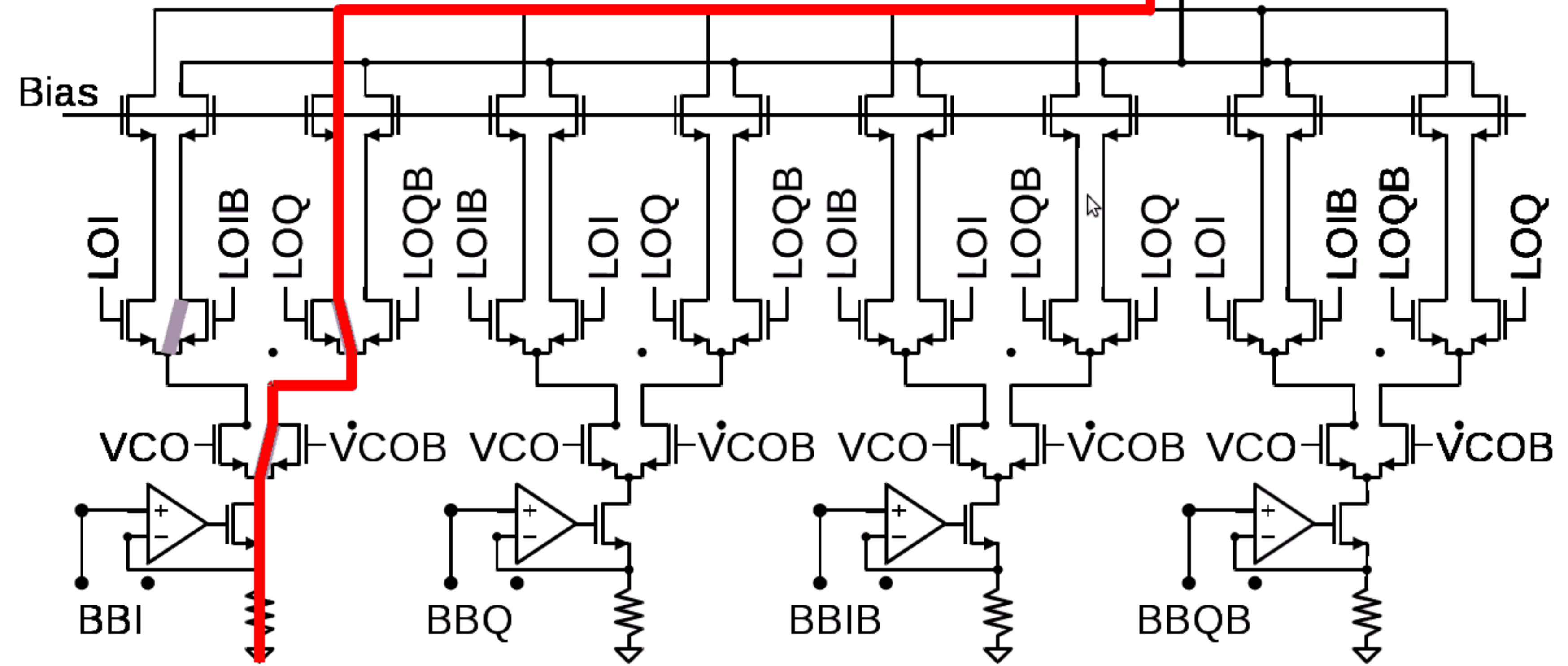
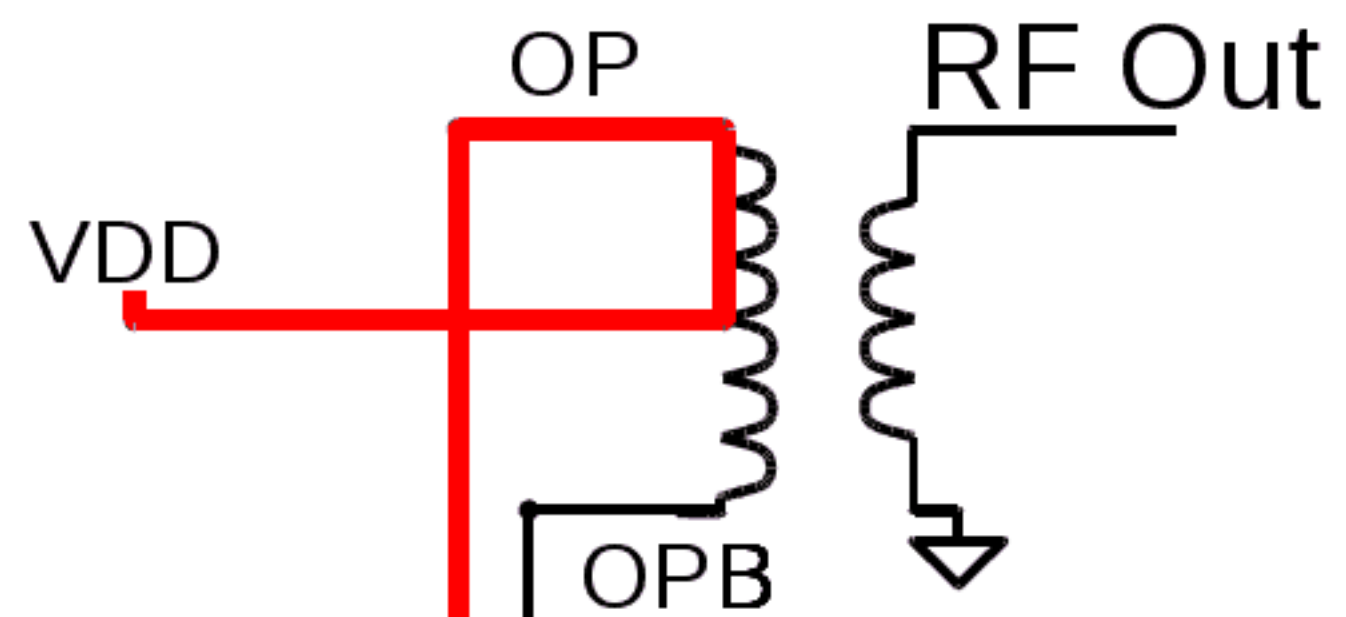
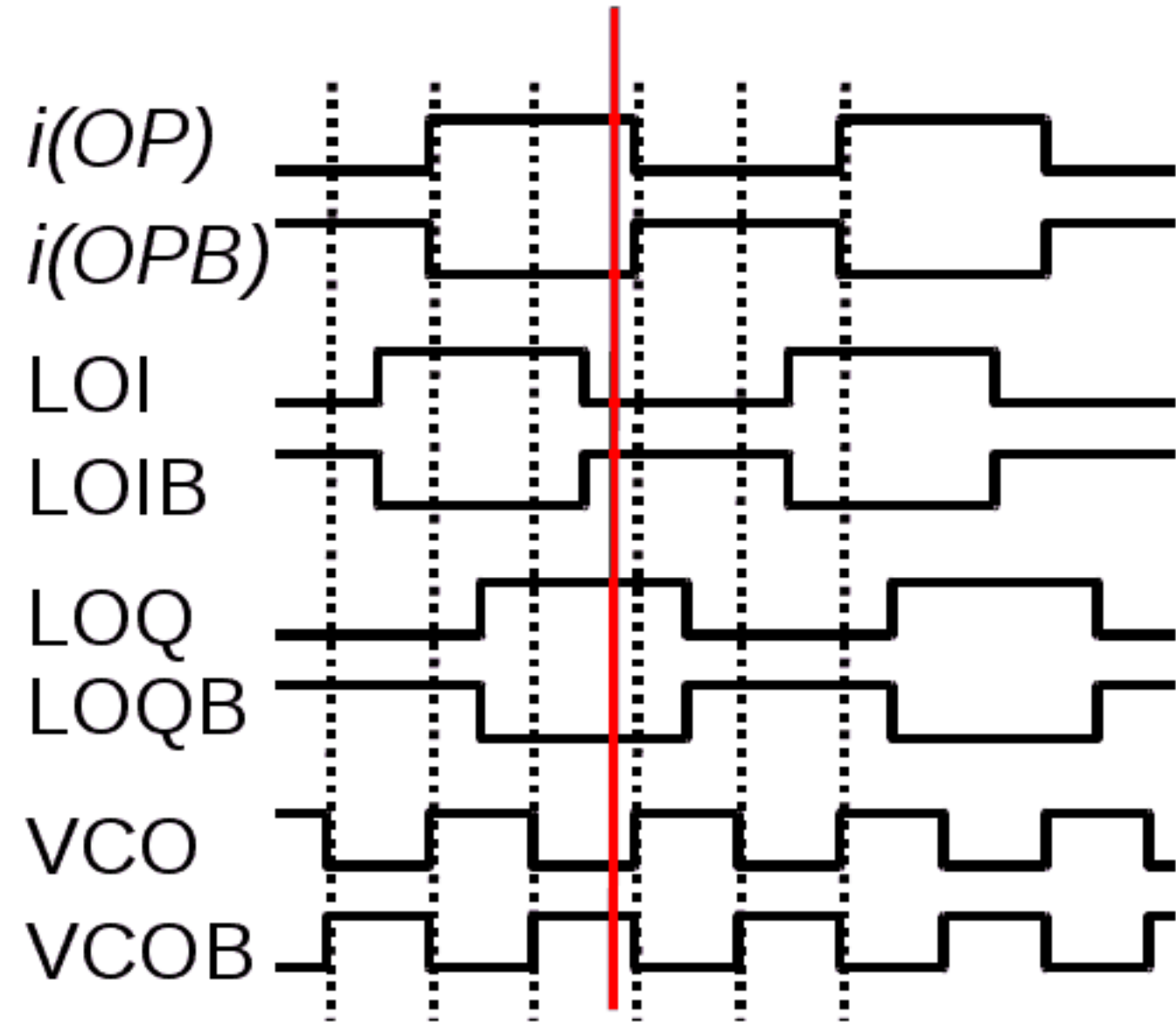
Switching Sequence



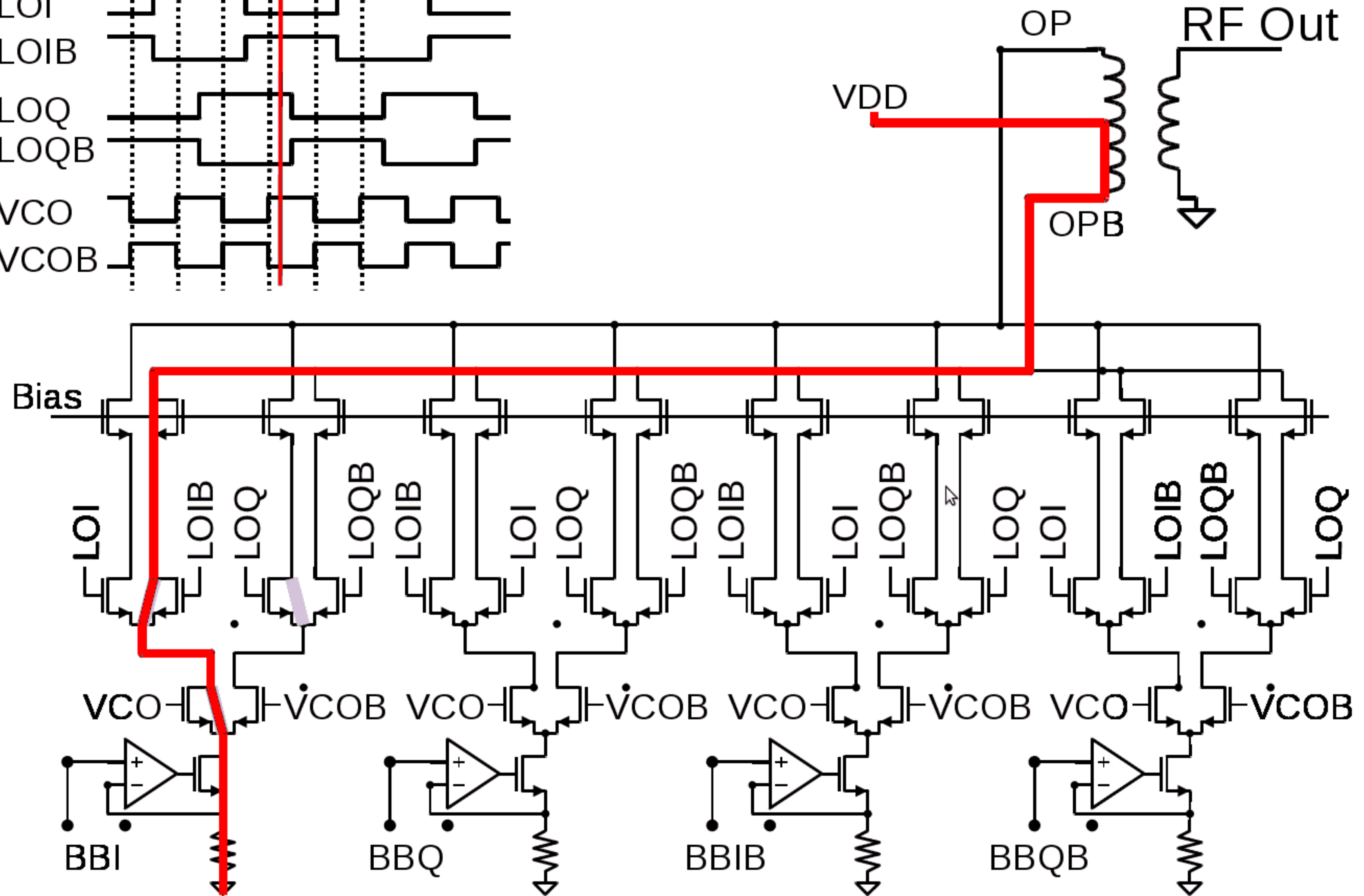
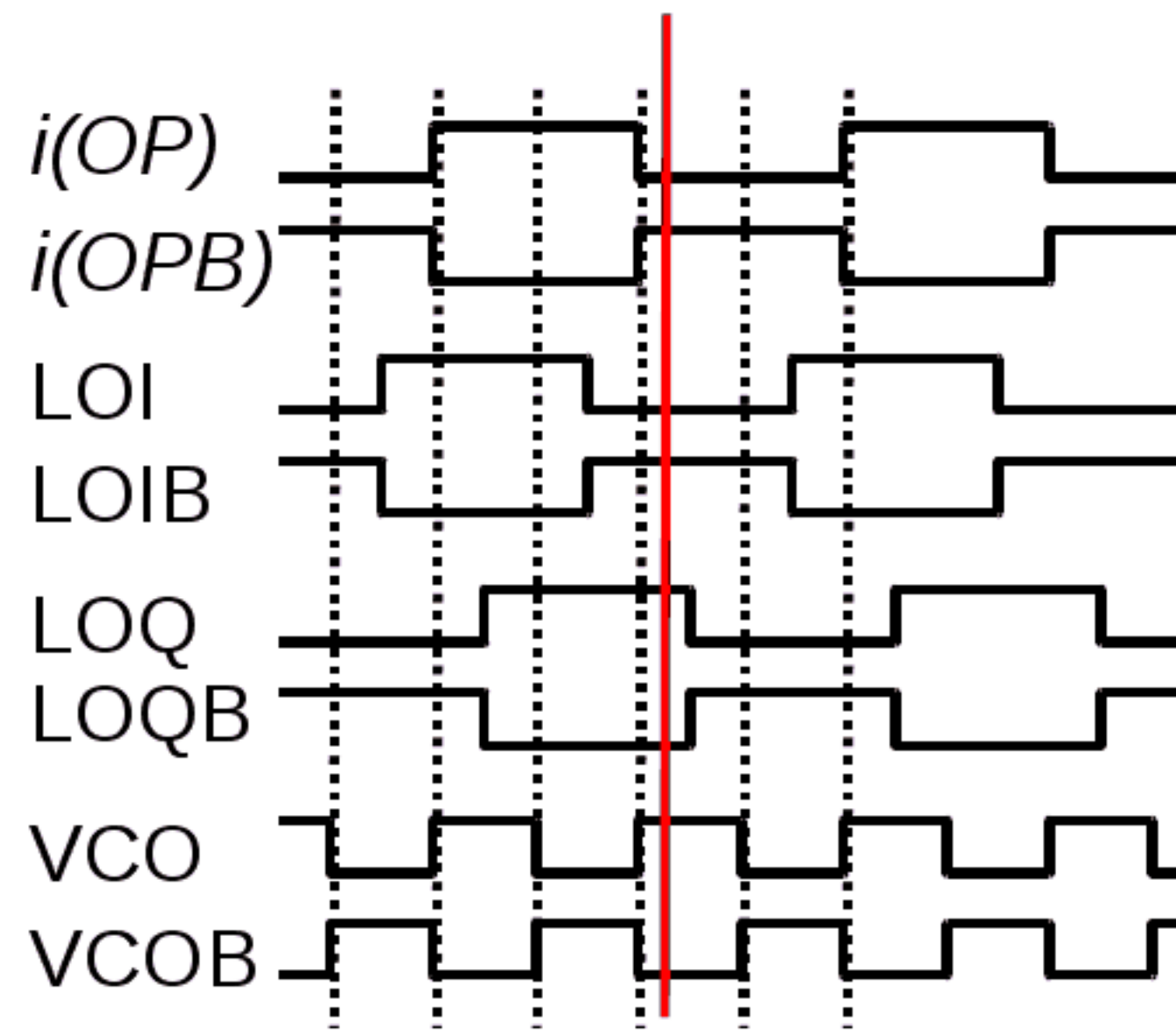
Switching Sequence



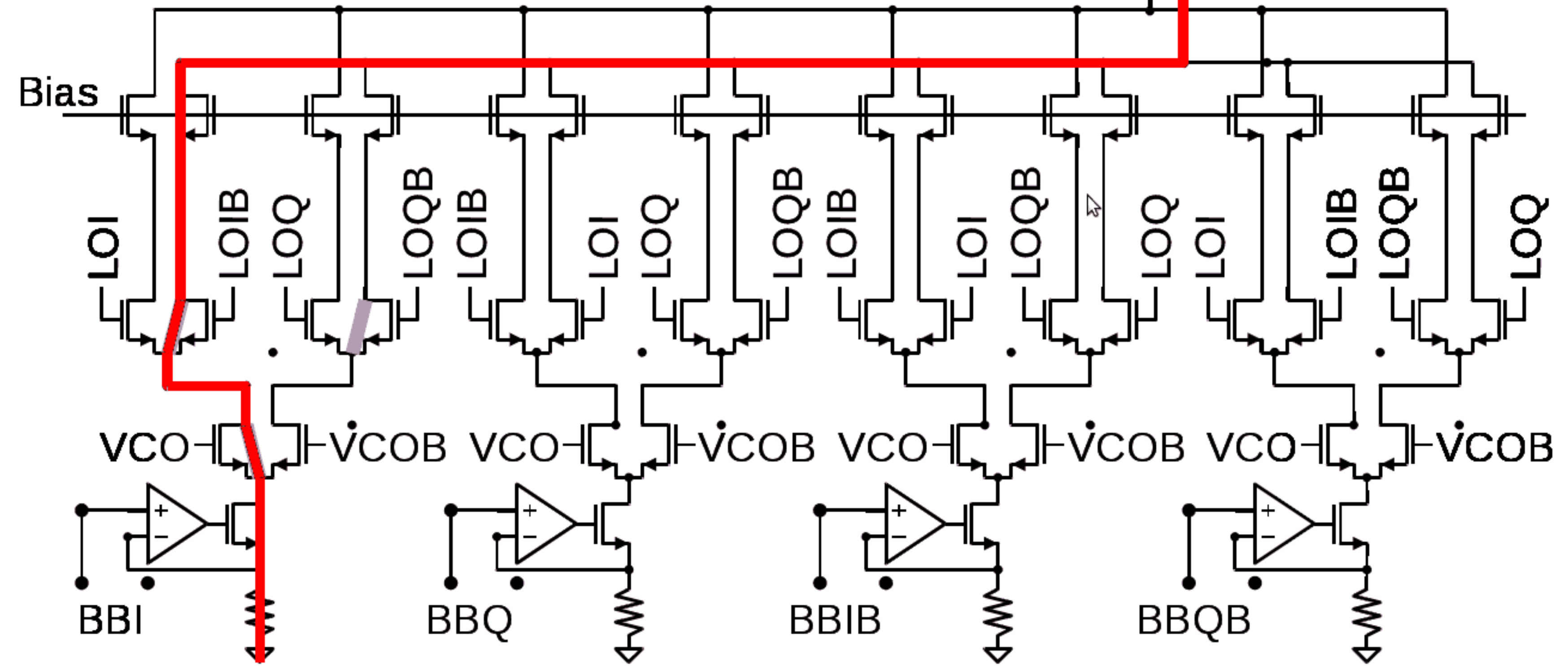
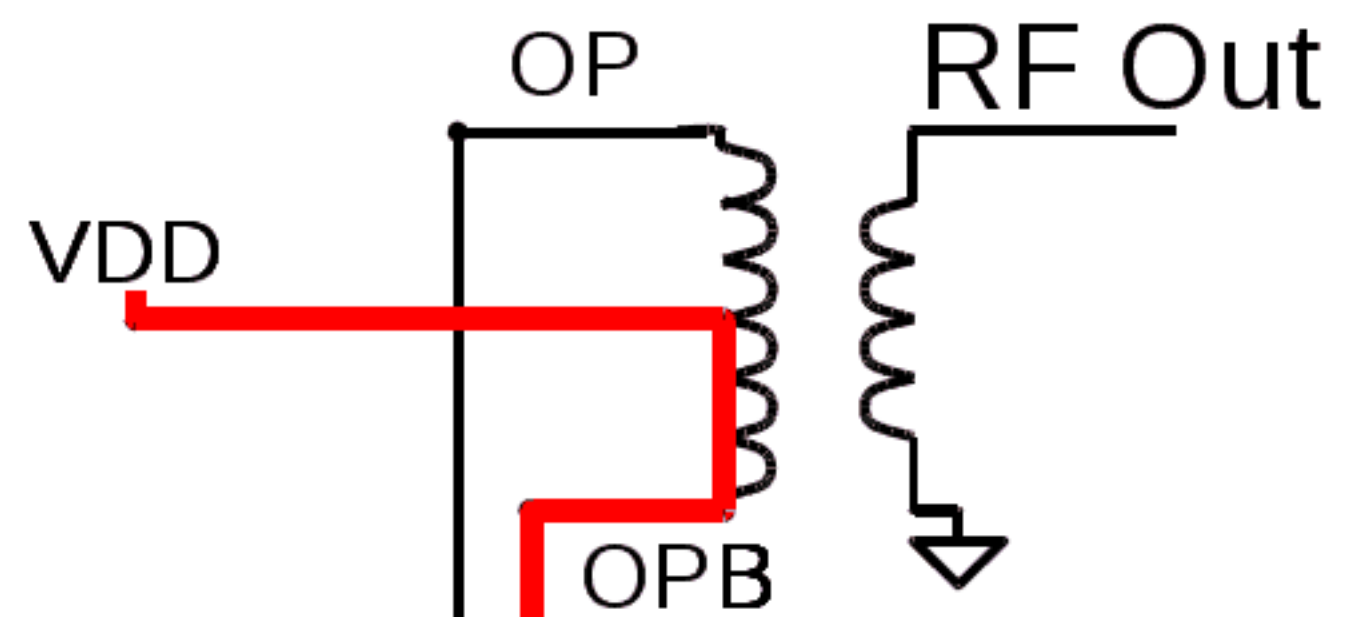
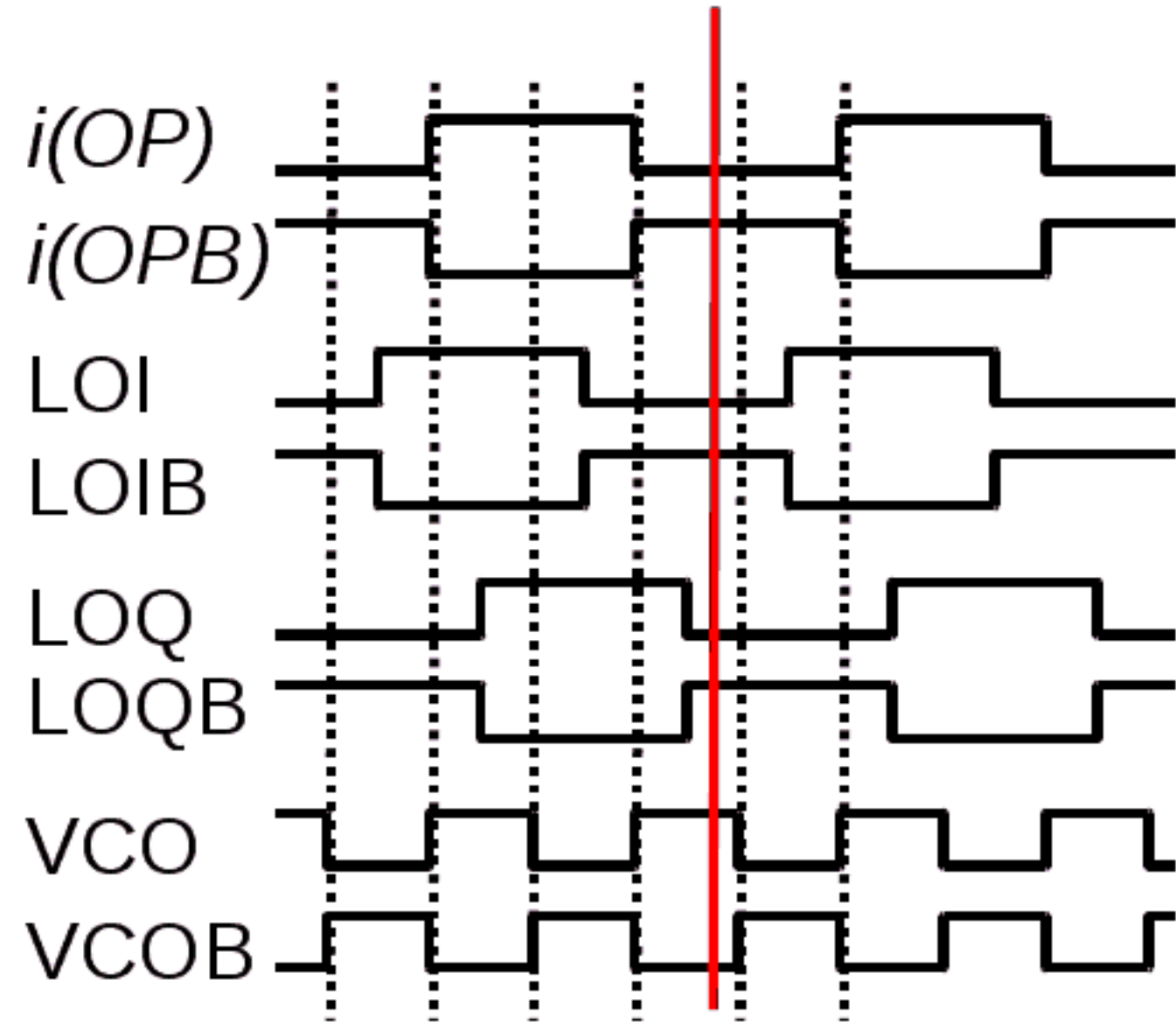
Switching Sequence



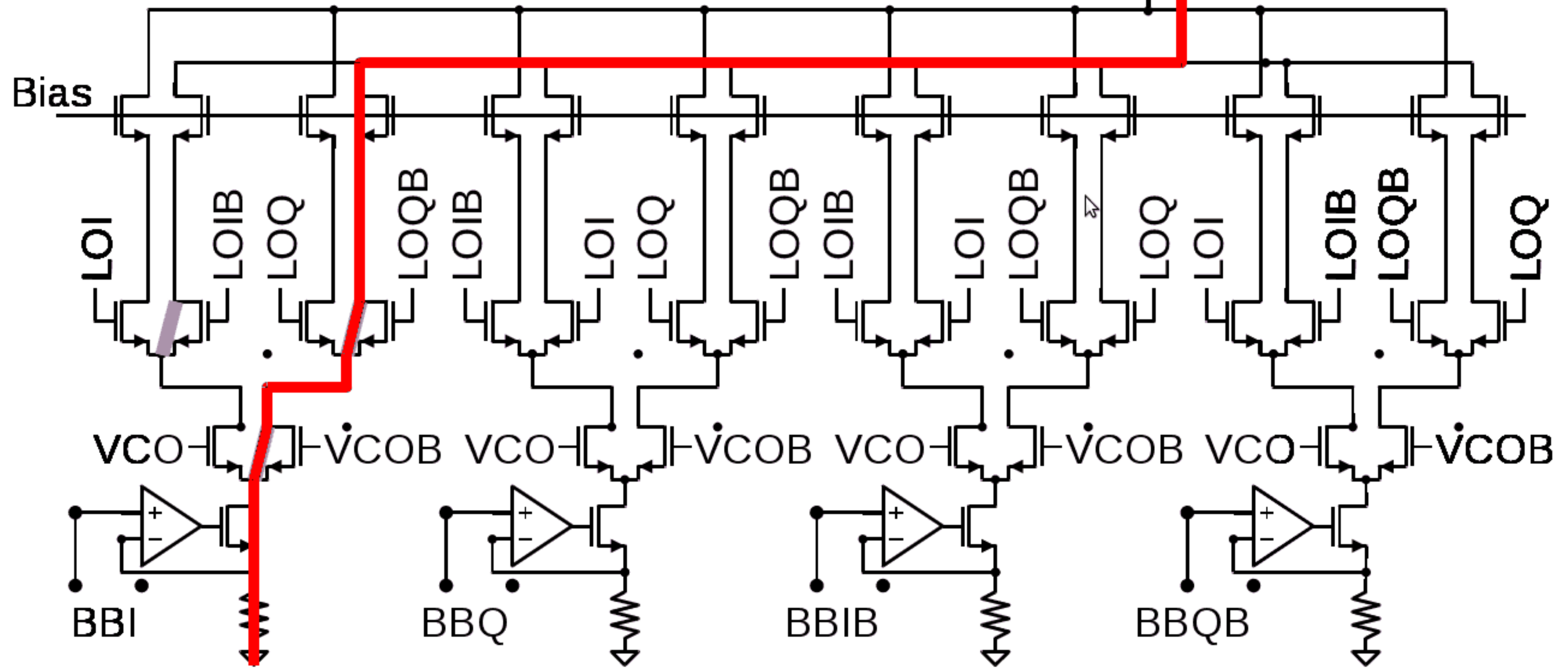
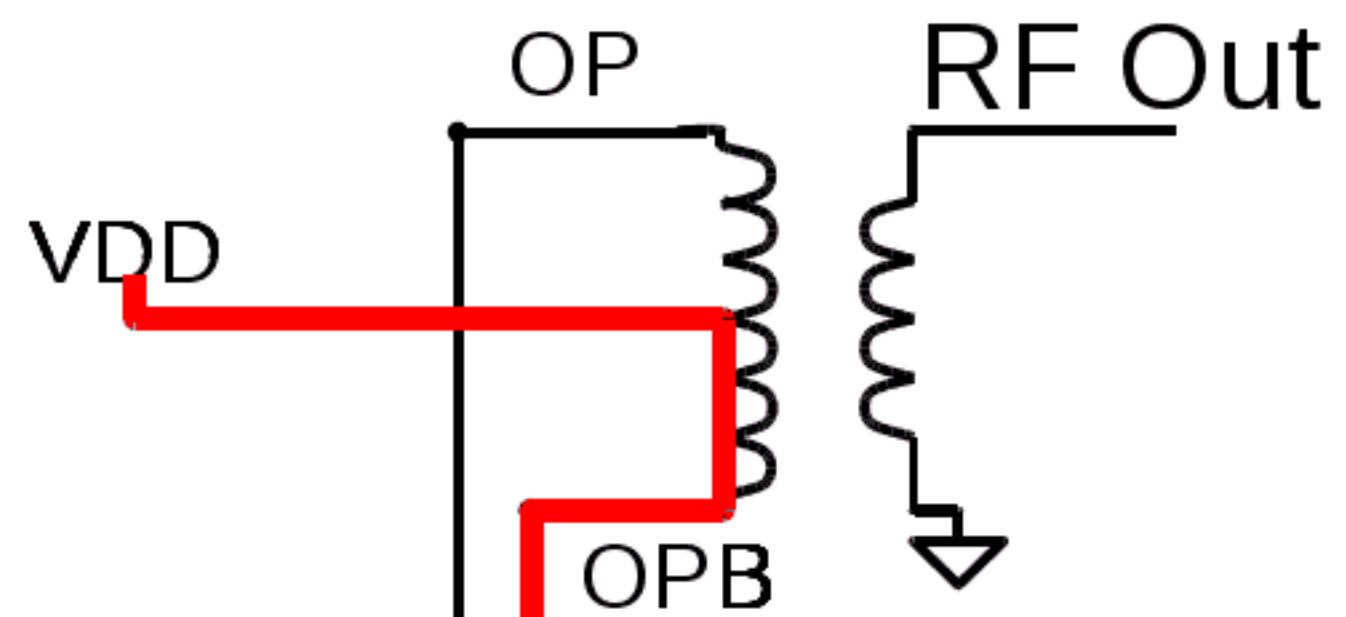
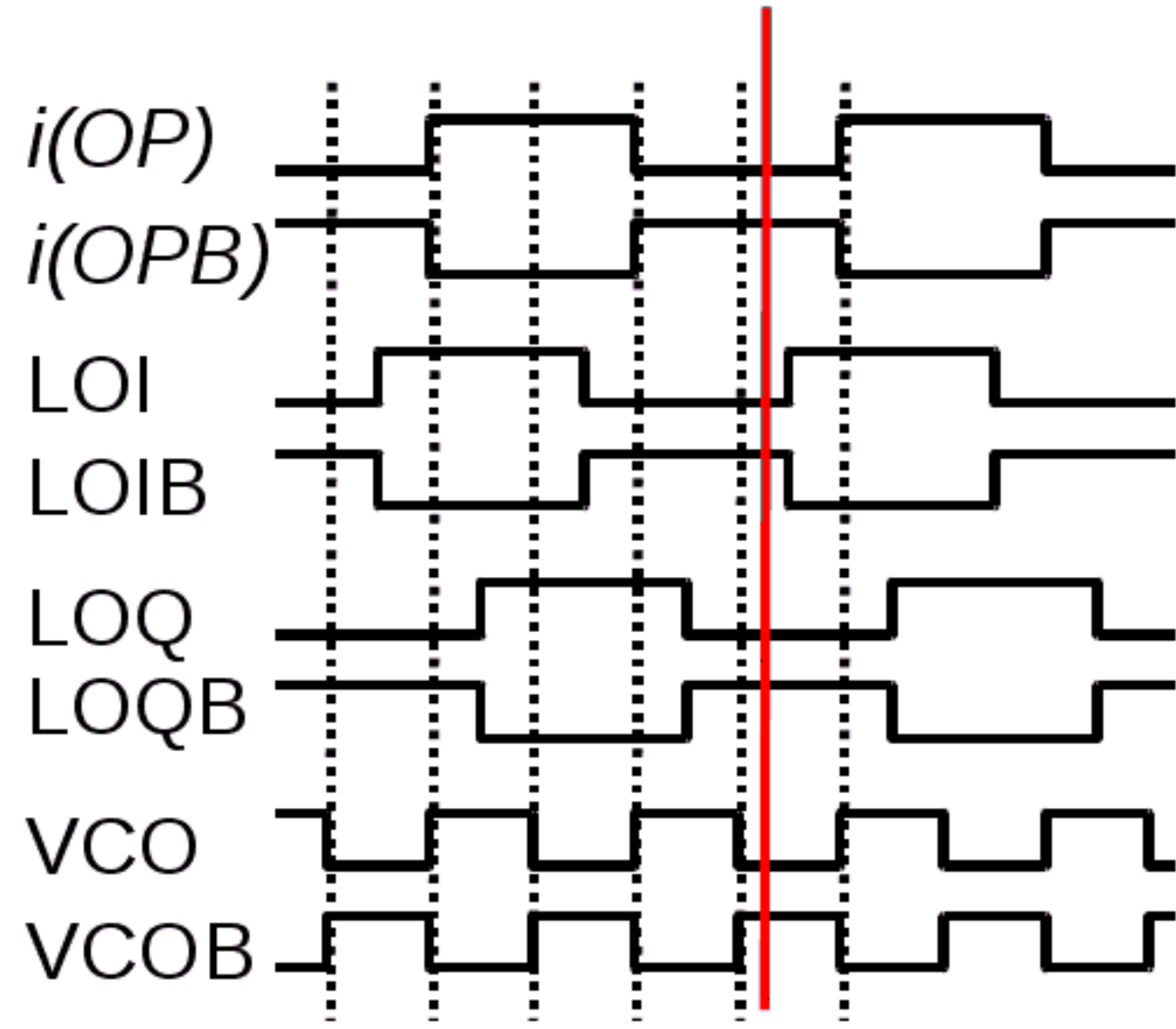
Switching Sequence



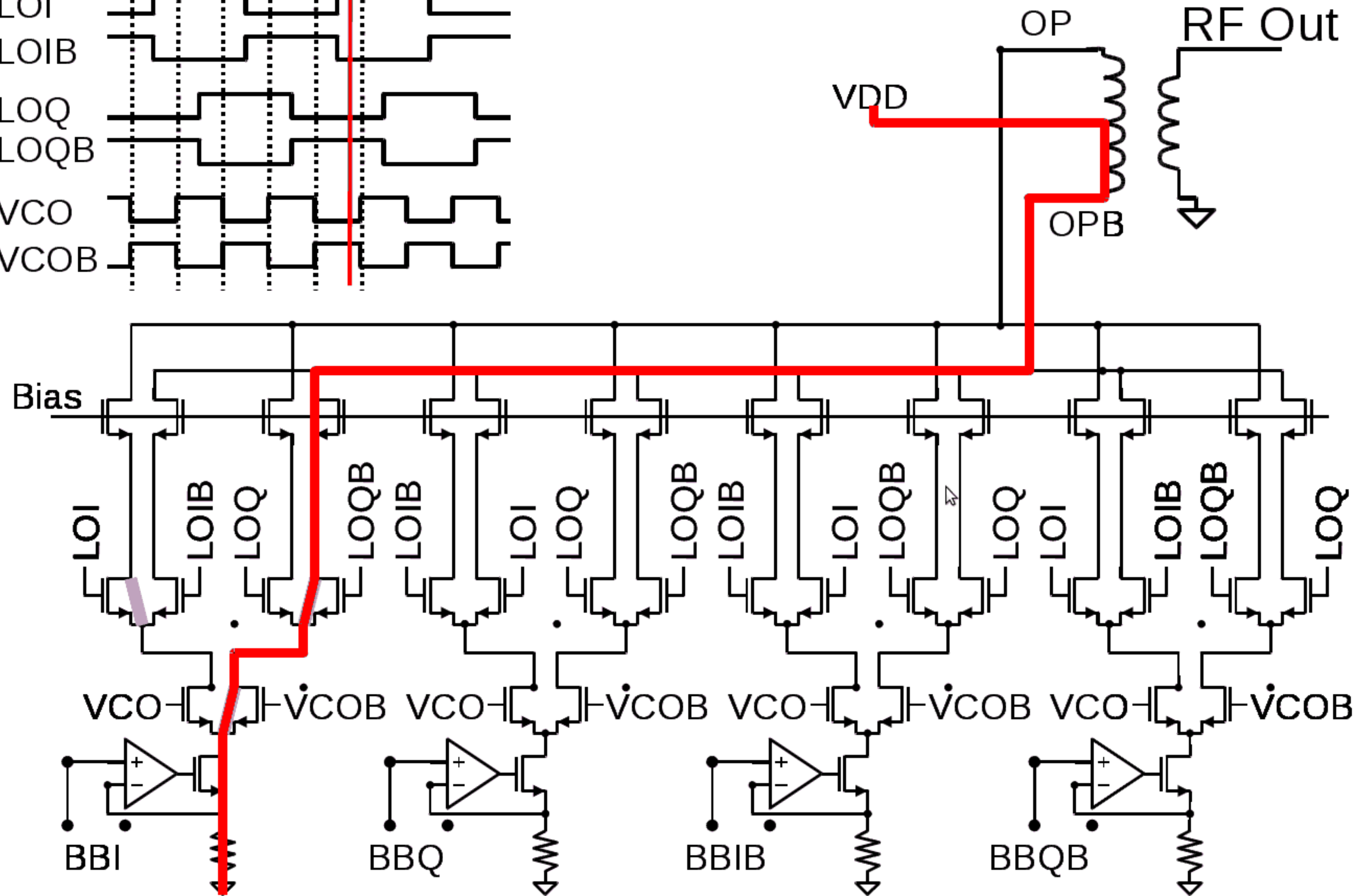
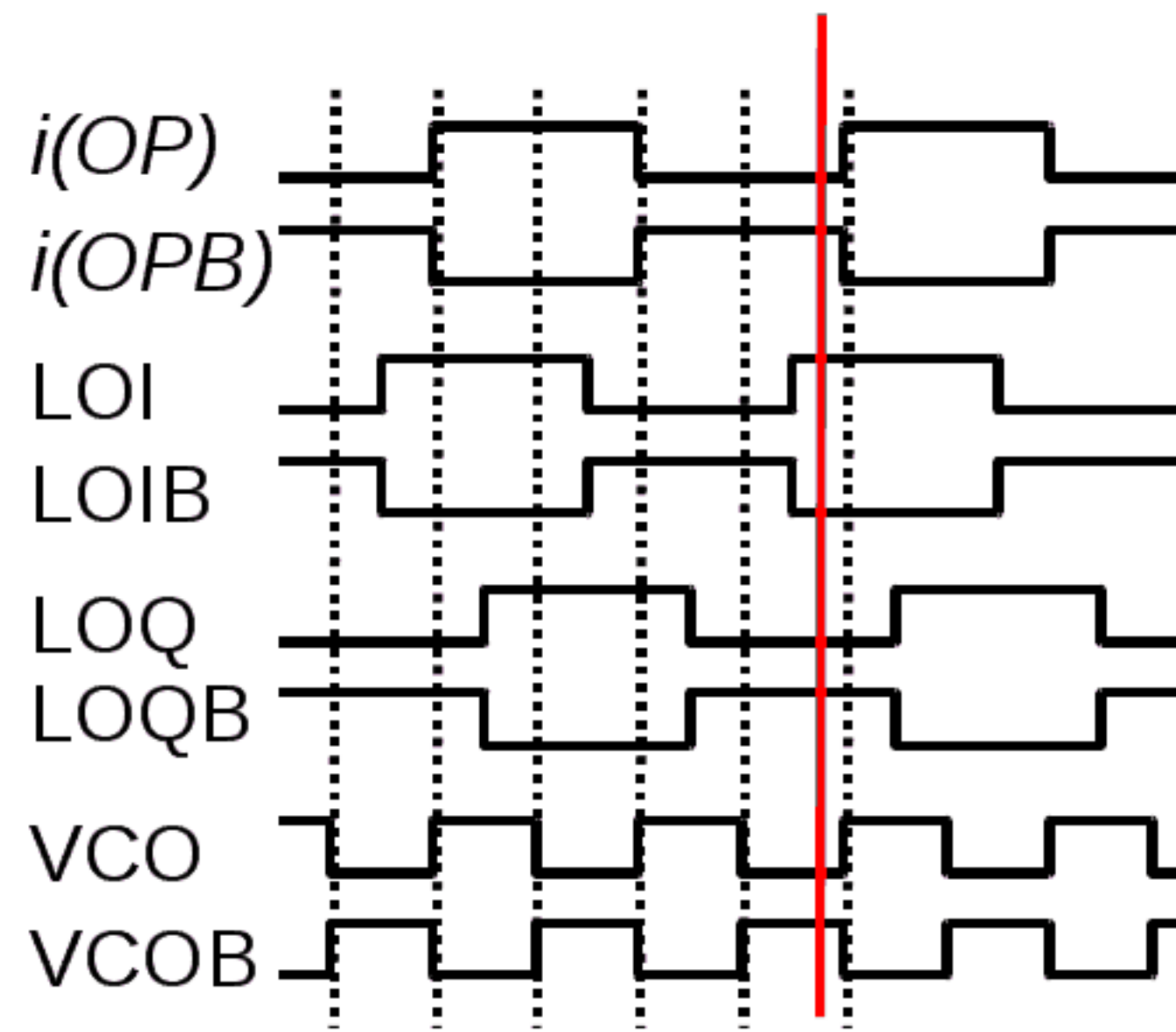
Switching Sequence



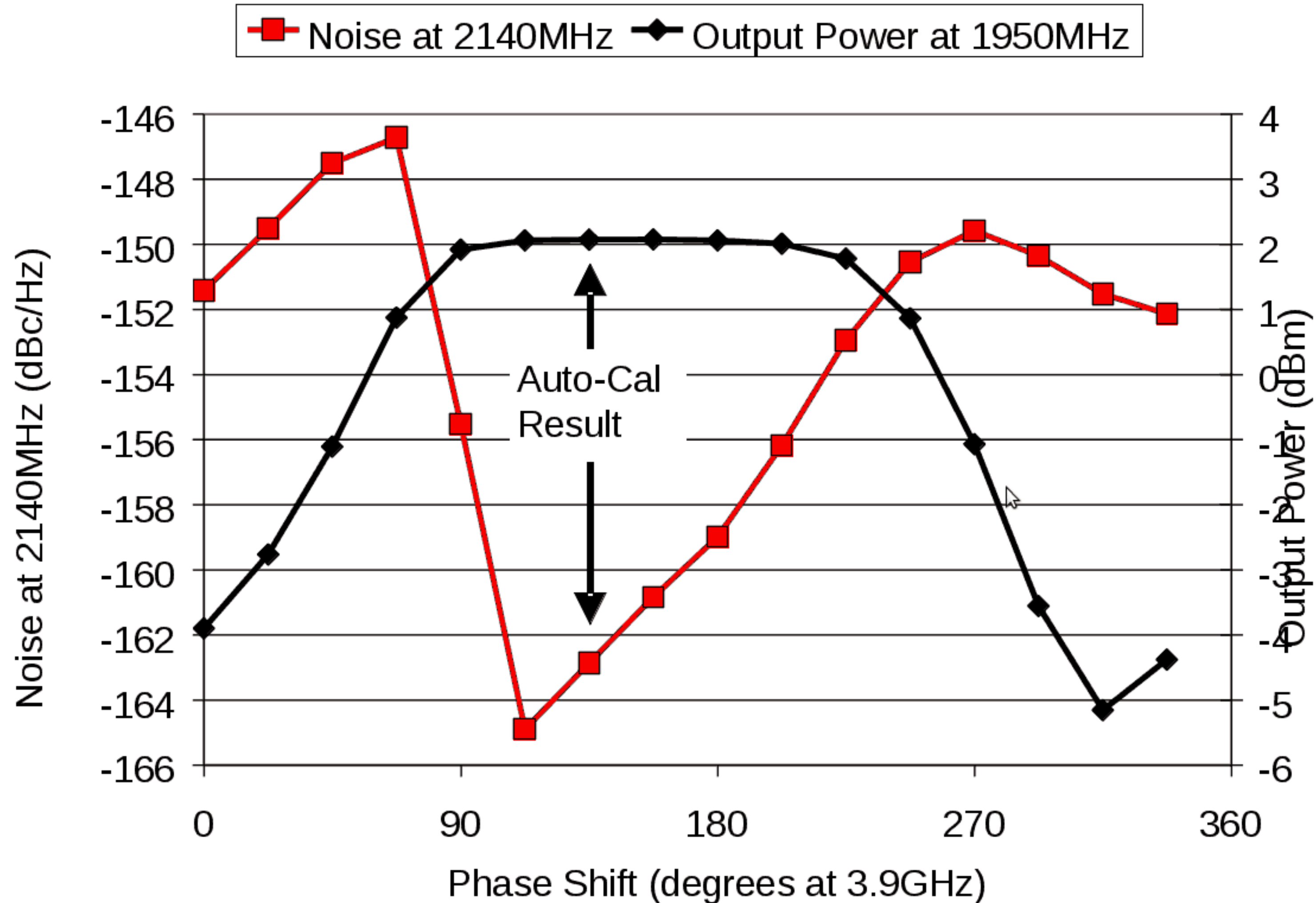
Switching Sequence



Switching Sequence

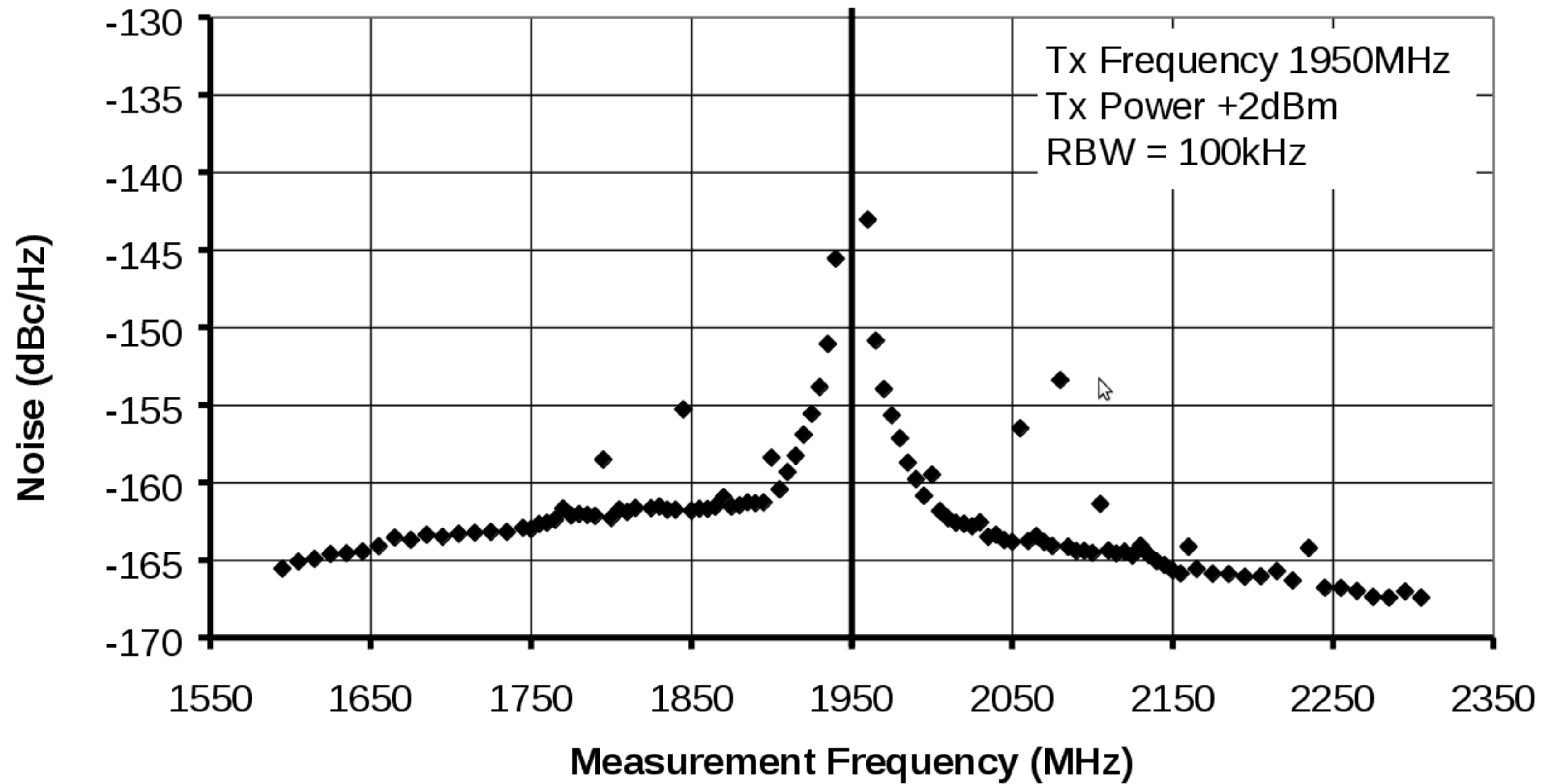


Effect of LO Phase Alignment to VCO



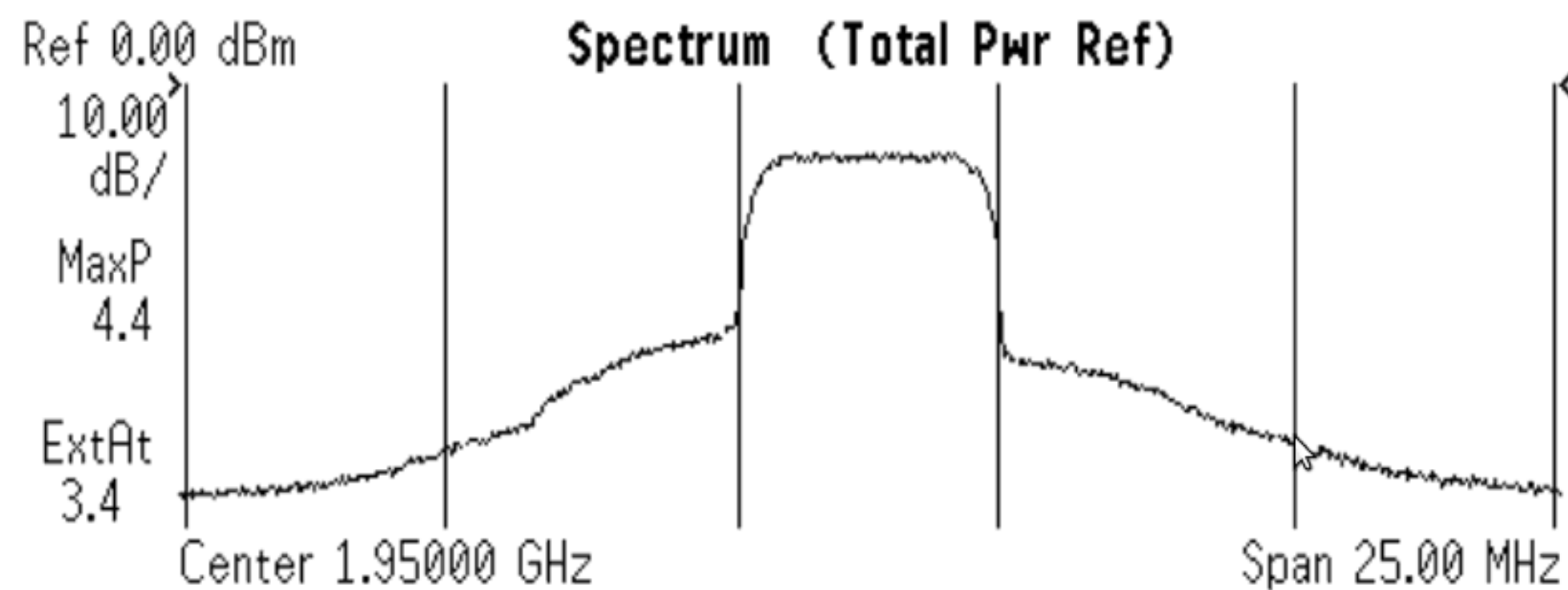
Typical Noise Performance

Noise vs. Frequency



Typical ACLR Performance

MS Ch Freq 1.95000 GHz Src:Input
ACPR-SWP: RRC Filter On 3GPP Averages: 1

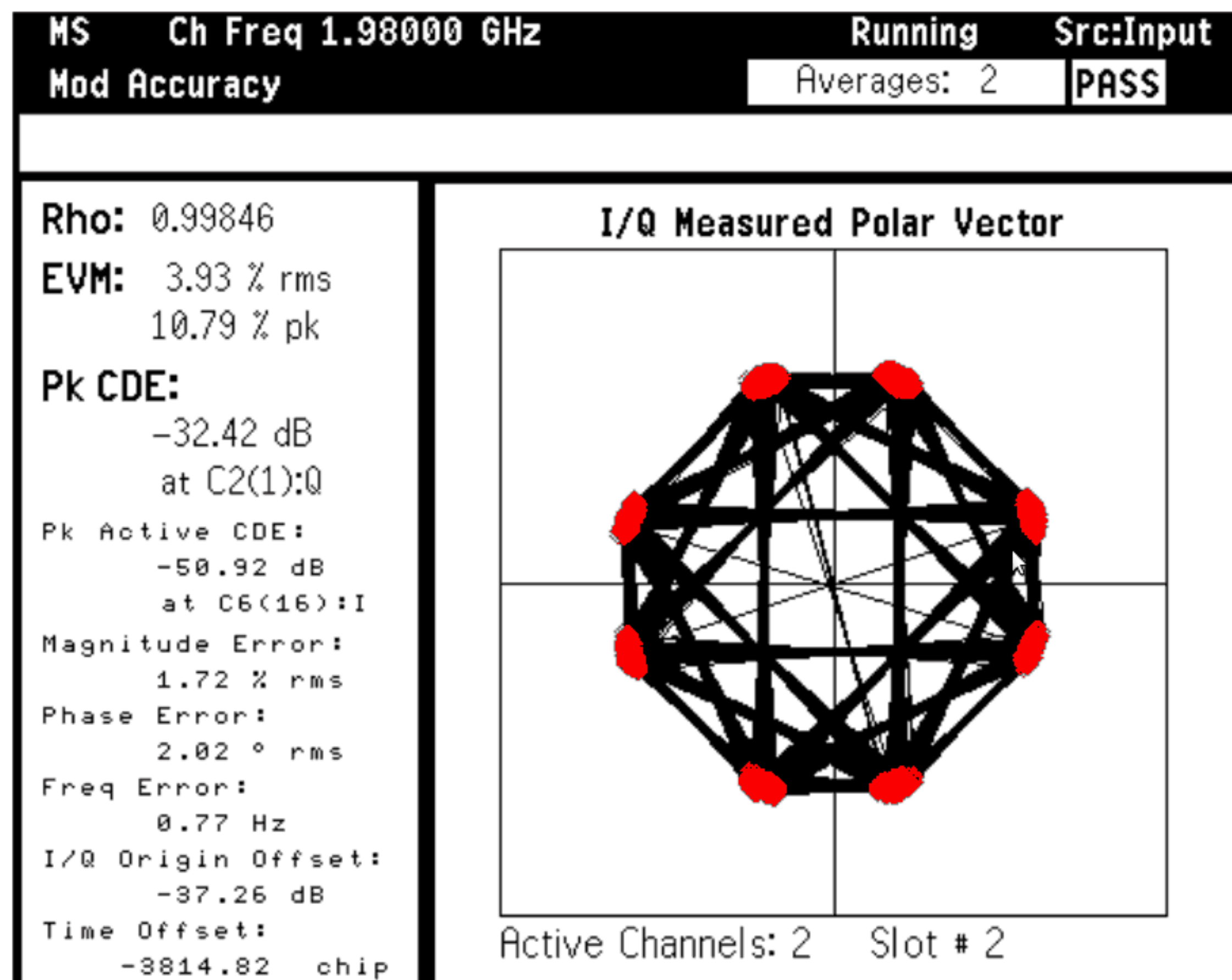


Total Pwr Ref: 3.77 dBm/ 3.84 MHz

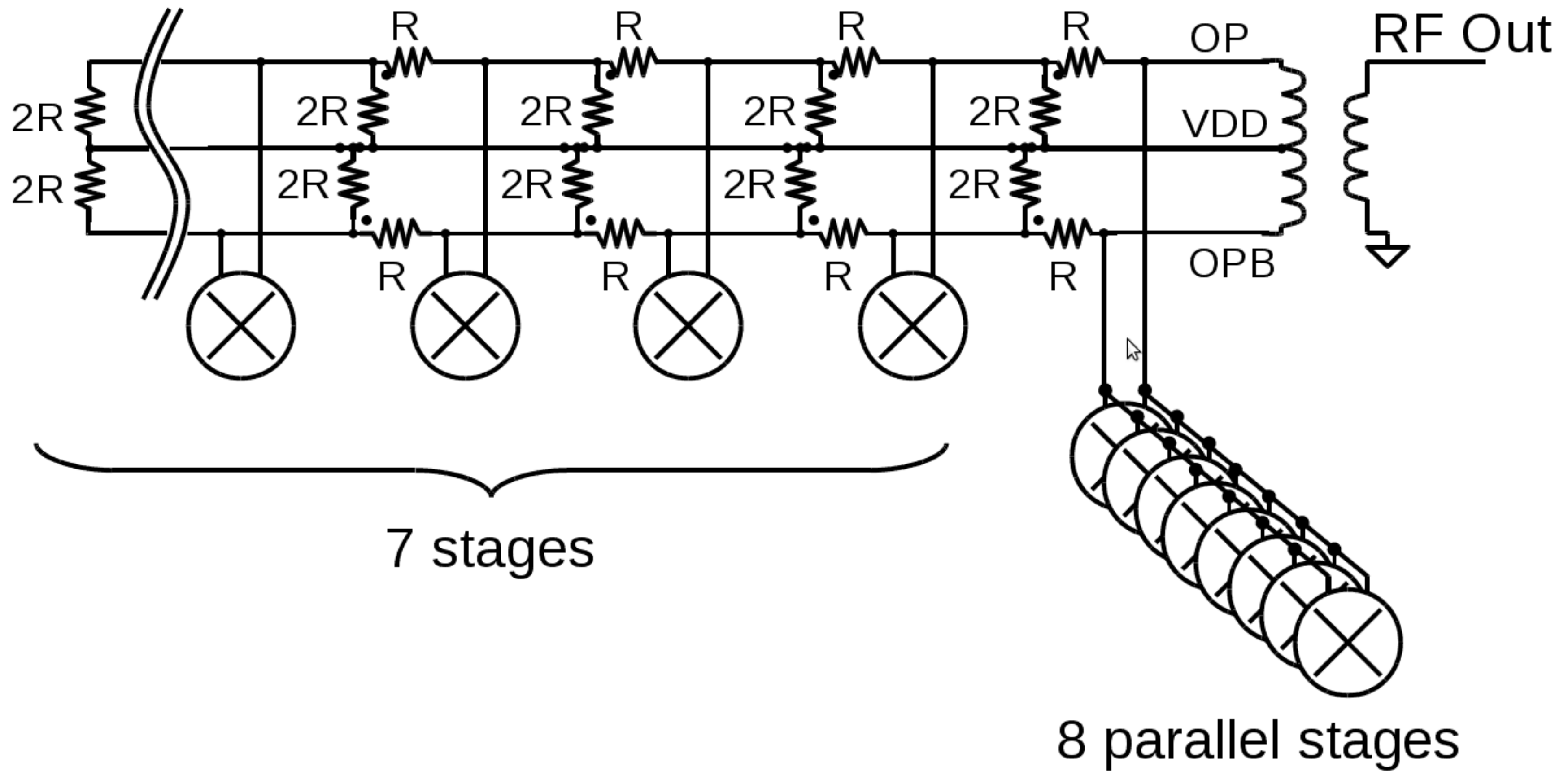
ACPR-SWP: RRC Filter On

Offset Freq	Integ BW	Lower		Upper	
		dBc	dBm	dBc	dBm
5.00 MHz	3.84 MHz	-46.33	-42.56	-50.84	-47.08
10.00 MHz	3.84 MHz	-72.48	-68.72	-70.68	-66.92

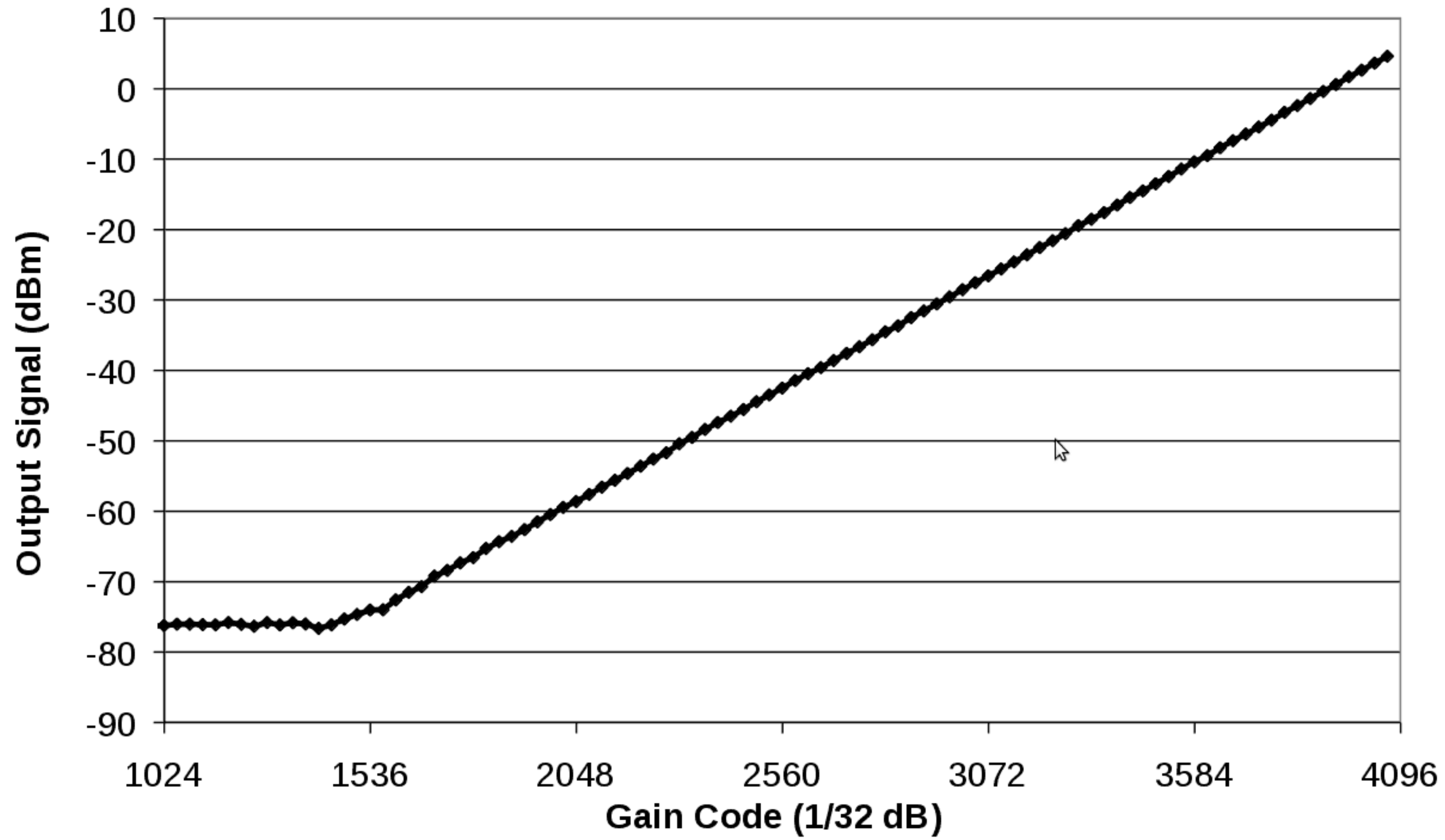
Typical EVM Performance



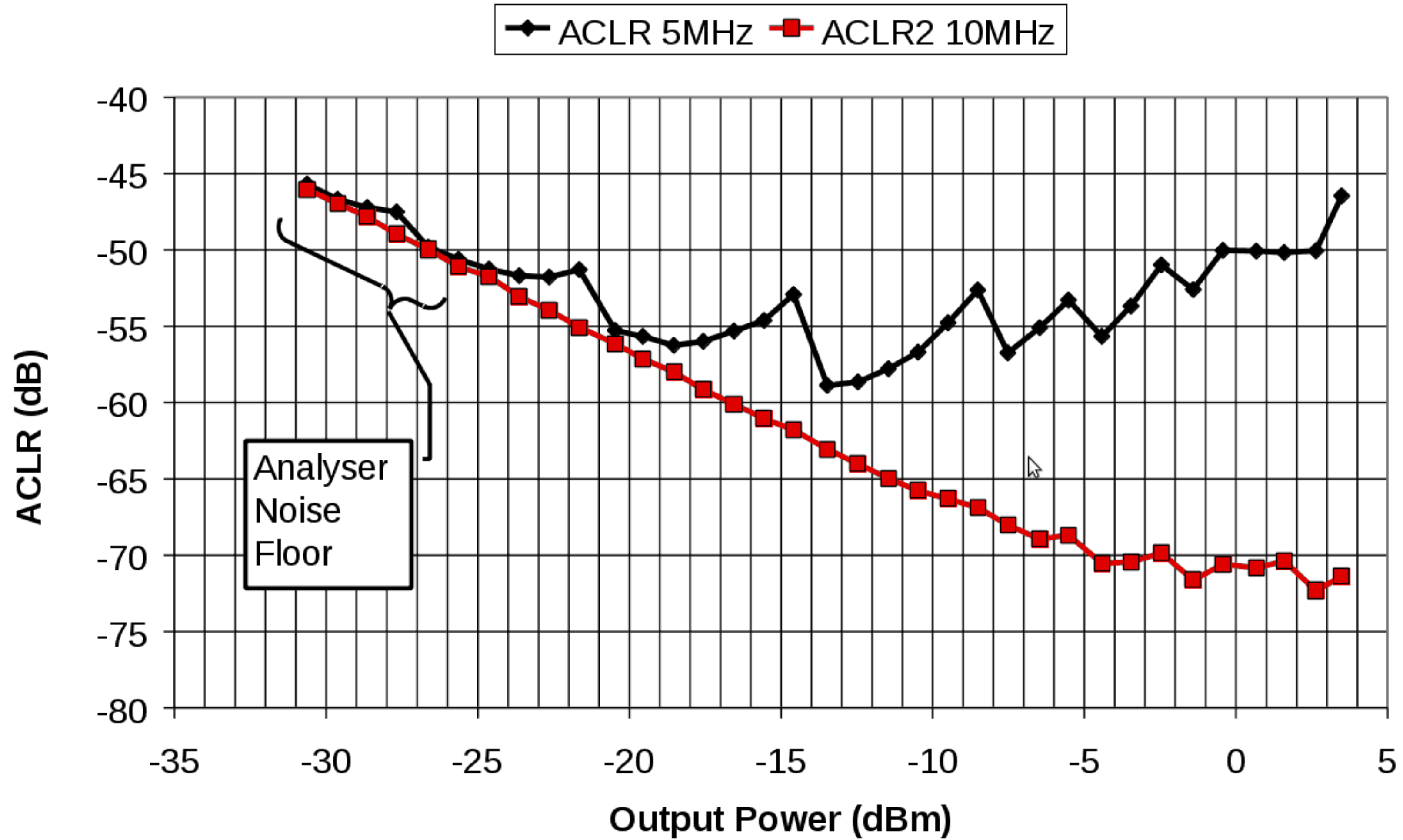
Gain Control



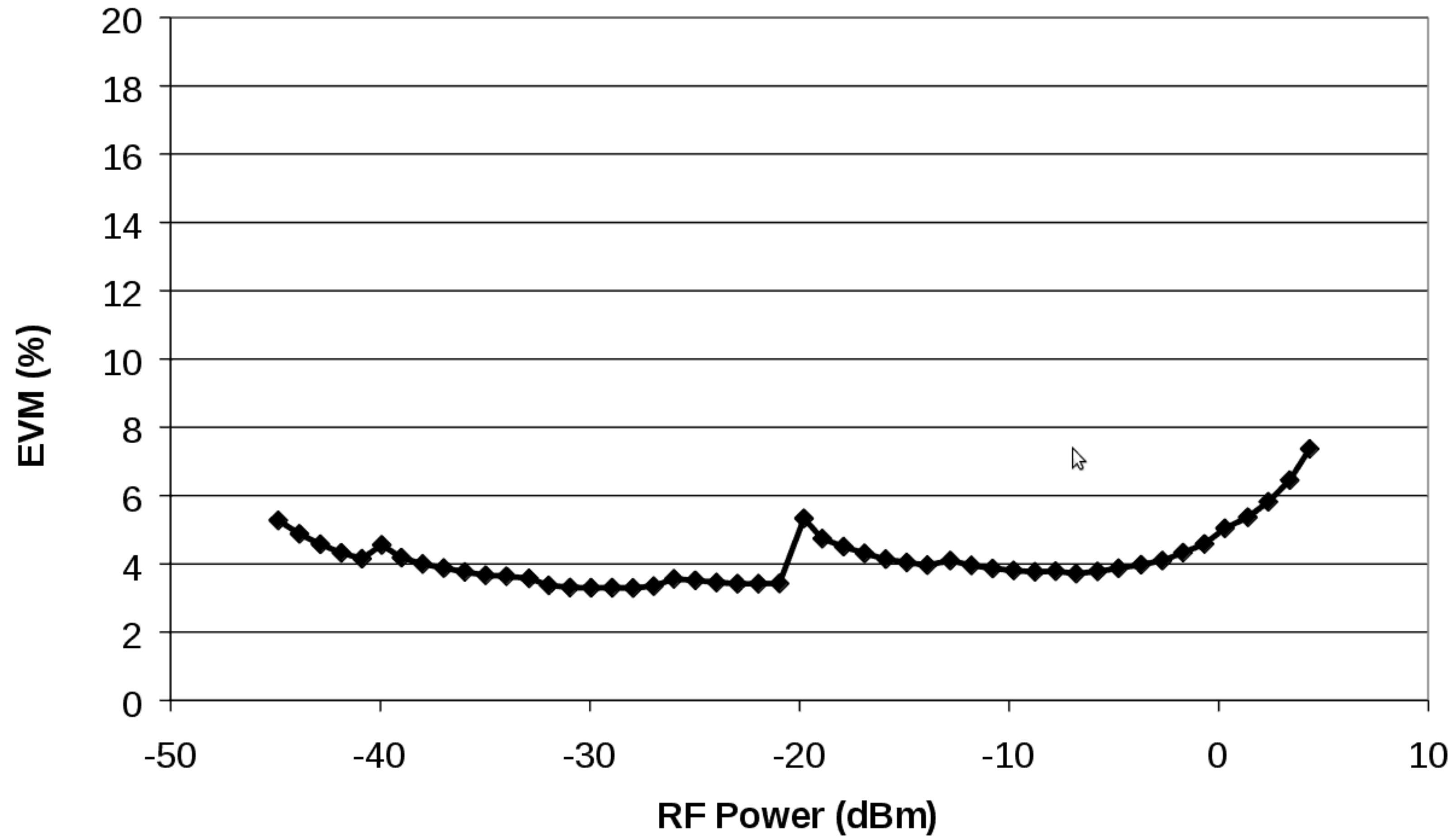
Gain Control Range



ACLR vs. RF Power

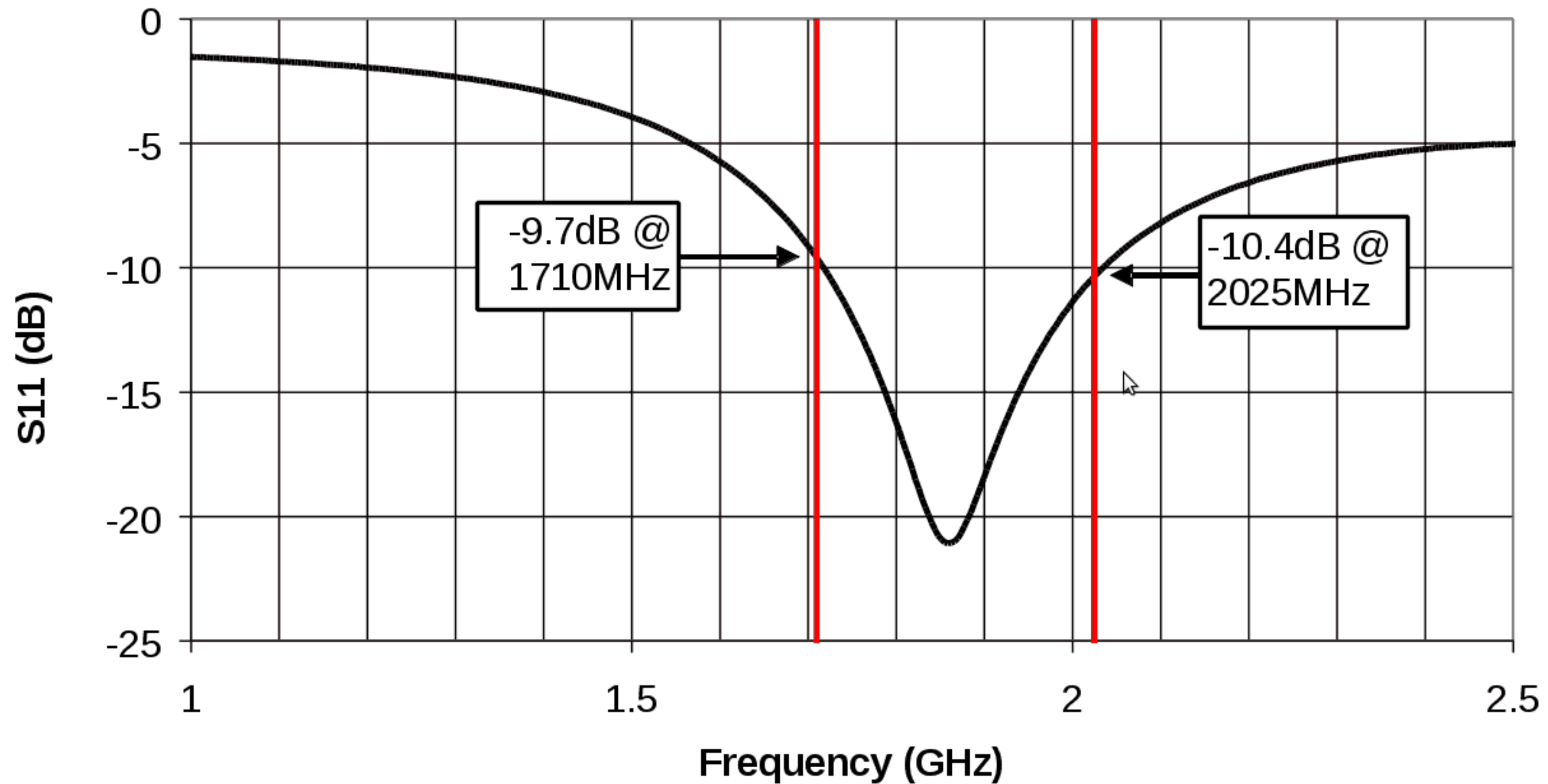


EVM vs. RF Power

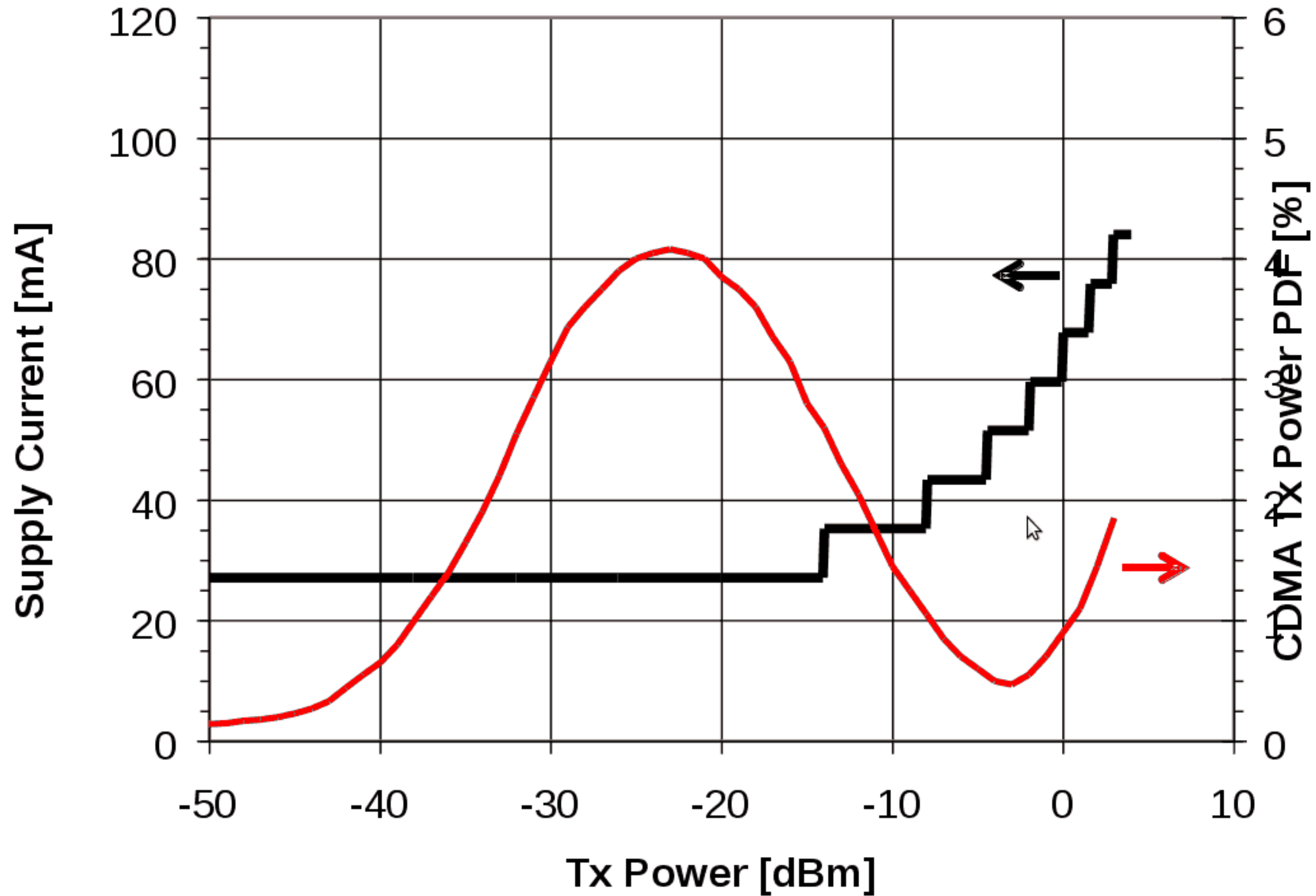


Output Match

Return Loss looking into Transmit IC Output Port

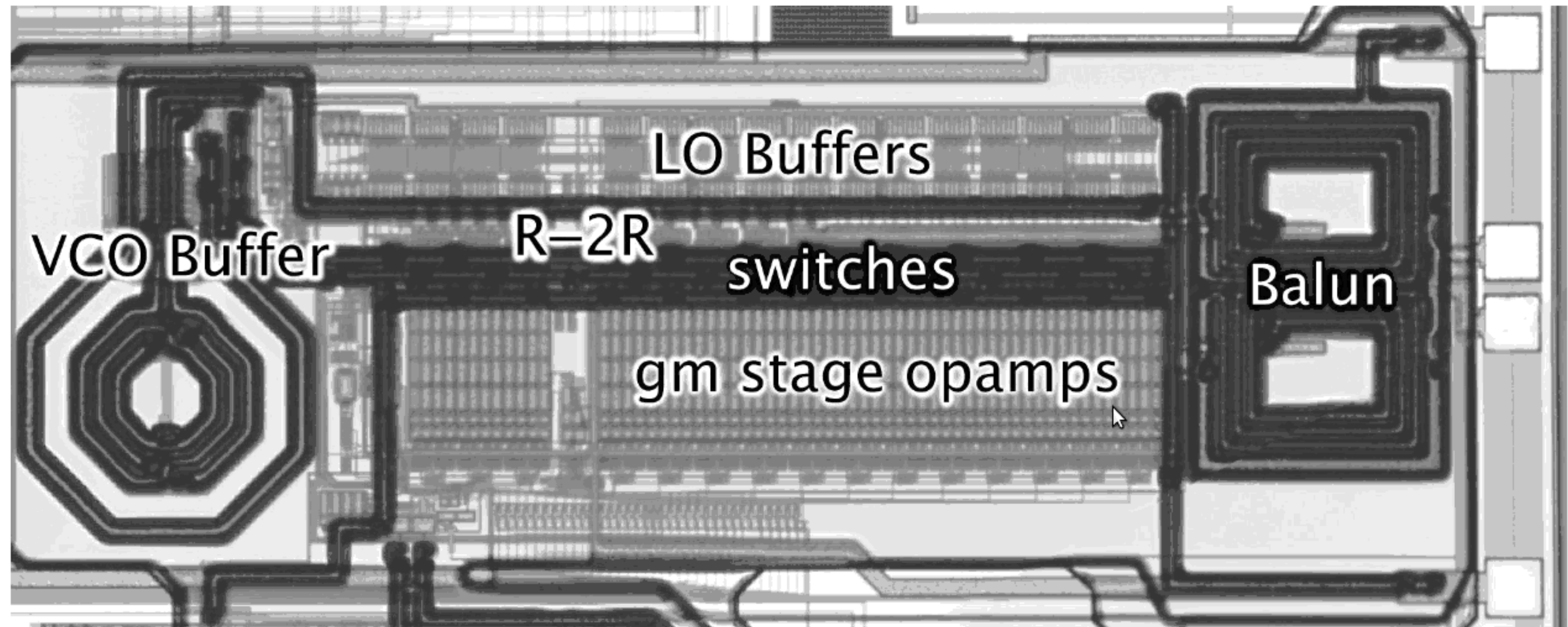


Supply Current



(Includes VCO buffer and LO path, but not VCO and synthesizer)

Die Photograph



0.8 mm² in 0.18μm CMOS

Performance Summary

Design	Process	Power [dBm]	ACLR [dBc]	Rx Noise [dBc/Hz]	Supply [V]	Current [mA]
Brenna et al ISSCC 2003	0.13 μ m CMOS	2.5	-38	-152	1.5	18 – 45
Kaczman et al RFIC 2005	0.35 μ m SiGe	9.5	-46	-142	2.8	49 – 64*
Tomiyama et al RFIC 2006	0.18 μ m SiGe	0	-38	-141	1.8	31 – 53
Koller et al RFIC 2006	0.13 μ m CMOS	10.75	-44	-152	2.7	26 – 80*
This Work	0.18μm CMOS	3.8	-46	-163	2.8	27 – 84

* Includes synthesizer and VCO